MARKED-UP COPY

SPECIFICATION

A SPIN TRANSISTOR BASED ON THE SPIN-FILTER EFFECT, AND ~~A~~ ~~NONVOLATILE~~NON-VOLATILE MEMORY USING SPIN TRANSISTORS

TECHNICAL FIELD

The present invention relates to a novel transistor~~. More specifically, the present invention relates~~, and more particularly to a transistor ~~having an~~the output ~~characteristic depending~~characteristics of which depend on the direction of ~~the~~ spin of ~~carriers~~a carrier, and to a nonvolatile memory circuit (nonvolatile memory) ~~using~~utilizing the ~~same~~transistor.

BACKGROUND ART

~~As a~~Conventionally, semiconductor ~~memory used in electronic equipment typified by a microcomputer, a DRAM (Dynamic Random Access Memory) has been mainly used~~memories used in electronic devices such as microcomputers have mainly employed dynamic random access memories (DRAMs) from the viewpoint of operating speed and the degree of device integration. ~~In the DRAM, it is difficult to respond to a request to save energy and mobile equipment in recent years due to the problems that energy is consumed for holding memory and the stored contents are lost when turning off the power. To respond to such request, essential is a novel memory having a nonvolatile characteristic in addition to high speed, high integration and low power consumption characteristics.~~ It is difficult, however, for DRAMs to accommodate the recent demands for lower energy consumption and mobility because DRAMs consume energy for memory storage purposes and the stored data is lost once power supply is turned off. In order to address such demands, a novel memory is required that is nonvolatile as well as fast, highly integrated, and energy-saving.

~~Attention is being focused on an MRAM (~~Magnetoresistive ~~Random Access Memory)~~random access memories (MRAMs) are now gaining attention as a next-generation memory ~~which can realize~~with the nonvolatile property, in addition to being capable of achieving operating speeds and levels of integration ~~equal~~comparable to those of ~~the DRAM and has a nonvolatile characteristic.~~DRAMs. The MRAM stores information ~~according to the directions of magnetization of ferromagnetic substances and electrically reads the information according to the directions of magnetization by~~in terms of the direction of magnetization of a ferromagnet. The relative magnetization configuration of the information stored in the MRAM is electrically sensed utilizing the giant magnetoresistance effect ~~of~~in a spin valve ~~device~~element, or the tunneling magnetoresistance (TMR) effect ~~of~~in a magnetic tunnel junction (MTJ). ~~The MRAM which uses the ferromagnetic substances~~ Since MRAMs utilize a ferromagnet, they can hold information in a nonvolatile manner without consuming energy.

~~FIGS. 17(A) and 17(B) are diagrams showing~~Fig. 17 shows a typical cell ~~structure~~configuration of an MRAM ~~using an~~utilizing a MTJ. As shown in ~~FIG~~Fig. 17(A), ~~in~~ the MRAM~~,~~ comprises a ~~one~~ 1-bit memory cell ~~is constituted by~~consisting of one MTJ and one metal oxide semiconductor (MOS ~~(Metal Oxide Semiconductor~~) transistor. The

gate of the MOS transistor is connected to a ~~read word line~~wordline for sensing, the source ~~thereof~~ is grounded, and the drain ~~thereof~~ is connected to one end of the MTJ~~, and the~~. The other end of the MTJ is connected to a ~~bit line~~bitline.

As shown in ~~FIG~~Fig. 17(B), the MTJ has a tunnel junction structure ~~having a thin insulator film interposed between two ferromagnetic electrodes and has~~consisting of two ferromagnetic electrodes separated by a thin insulating film. The MTJ provides the TMR effect in which tunnel resistance ~~is different according to the relative directions of magnetization of the two ferromagnetic electrodes. In particular, the rates of change of the TMR when the two ferromagnetic electrodes have parallel magnetization and when they have anti parallel magnetization are called a TMR ratio which is used for evaluating the TMR effect.~~

~~The MRAM stores information by allowing the magnetization state of the MTJ, that is, the relative directions of magnetization of the two ferromagnetic electrodes to be parallel magnetization or anti parallel magnetization by a synthesized magnetic field induced by electric currents flowed to a bit line and a rewrite word line, not shown, orthogonal thereto. To read stored information stored in a specified~~varies depending on the relative magnetization configuration of the two ferromagnetic electrodes. The rate of change of TMR between the case where the two ferromagnetic electrodes carry parallel magnetization and the case where they carry antiparallel magnetization is referred to as the TMR ratio, which is used for the evaluation of the TMR effect.

In the MRAM, information is stored in terms of the configuration of magnetization of the MTJ. Specifically, the relative magnetization configuration of the two ferromagnetic electrodes is rendered either parallel or antiparallel using a composed magnetic field formed by magnetic fields induced by currents that are caused to flow through the bitline and a wordline for writing (not shown) disposed perpendicular to the bitline.

When sensing information stored in a particular cell, a voltage is applied to a specified~~c read word line~~ wordline for sensing connected to the cell ~~to conduct~~so as to bring the MOS transistor~~, a read electric current (hereinafter, called a "driving current") is flowed from a specified bit line~~ into conduction, so that a current for sensing (to be hereafter referred to as a "drive current") flows through the MTJ via a specific bitline connected to the cell ~~to the MTJ, and the~~. A voltage dropped ~~of~~ across the MTJ ~~based on~~ due to the TMR effect is then detected as an output voltage to ~~read~~sense the stored information.

~~DISCLOSURE~~SUMMARY OF THE INVENTION

~~The MRAM using the MTJ employs the ferromagnetic substances to have nonvolatile, low power consumption, and high speed characteristics. The~~Because the MRAMs based on MTJ employ ferromagnets, they are nonvolatile, energy-saving, and fast. In addition, their simple cell structure ~~is simplified to be~~renders the MRAMs suitable for high -density integration. ~~The~~ However, before the MRAM ~~is expected~~can be realized as a next--generation nonvolatile memory~~. To realize this, there are~~, the following problems ~~to~~must be ~~solved~~overcome.

(1) ~~The~~An MTJ ~~has a binary~~exhibits two resistance value~~s~~ corresponding to ~~the magnetization states of parallel magnetization and anti parallel magnetization. The~~

~~MRAM flows the driving current to the MTJ to detect the resistance value~~parallel and antiparallel magnetization, and an MRAM detects these resistance values as ~~an output voltage. To~~output voltages by causing a drive current to flow through the MTJ. Thus, in order to obtain a high output voltage, the ~~thickness of the insulator film of the MTJ must be adjusted to optimize the tunnel resistance.~~tunnel resistance must be optimized by adjusting the thickness of the MTJ insulating film. However, ~~S~~since the TMR ratio also depends on the ~~thickness of the insulator film, optimizing~~insulating film thickness, optimization of the tunnel resistance is limited.

~~(2) To precisely read the memory contents of information, the TMR ratio must be large to increase the ratio of the~~(2) Further, if the stored information is to be sensed accurately, the TMR ratio must be increased such that a high ratio of output voltages of the two magnetization ~~states of~~configurations, i.e., parallel ~~magnetization and anti-parallel magnetization. To realize a high TMR ratio, ferromagnetic substances having large spin polarizability must be used to optimize the forming method, material and film~~and antiparallel, can be obtained. In order to achieve a high TMR ratio, a ferromagnet with a large spin polarization must be employed, and also the method of forming an insulating layer and its material and thickness ~~of the insulator layer~~, for example, must be optimized.

(3) In ~~the~~an MRAM ~~using the~~utilizing a MTJ, ~~a~~the bias applied to the MTJ must be ~~large~~increased in order to increase the operating speed. ~~The~~ However, the MTJ has ~~an unavoidable~~the fundamental problem ~~in principle that the TMR ratio is decreased when~~that, as the voltage drop ~~caused between~~across the ferromagnetic electrodes ~~is increased. The~~increases, the TMR ratio drops. Thus, the rate of change of ~~an output voltage based on the TMR is decreased as the voltage drop caused in the MTJ is increased. The phenomenon is due to~~output voltages due to TMR decreases as the voltage applied to the MTJ increases. This phenomenon is inherently based on the TMR effect ~~itself. It is difficult~~and hard to avoid ~~it~~ as long as the configuration of magnetization ~~states are read only~~is sensed based solely on the TMR effect.

~~Summarizing the above problems~~Thus, in order to detect ~~stored~~ information stored in a MTJ with high sensitivity ~~in the MTJ,~~, the output voltages must be optimized by adjusting the impedance (junction resistance) of the MTJ ~~must be adjusted to optimize the magnitude of output voltages. Further, the TMR ratio must be large~~. It is also necessary to increase the ~~ratio of the~~ output ~~signals of~~signal ratio of the two magnetization ~~states of~~configurations, namely, parallel ~~magnetization and anti-parallel magnetization. The bias resistance of the TMR ratio is necessary so as not to decrease the TMR ratio by a bias~~and antiparallel, by increasing the TMR ratio. At the same time, the TMR ratio must be prevented from being lowered by biasing.

~~If an~~All of the aforementioned problems can be overcome if output signal characteristics can be freely designed ~~by the~~in terms of peripheral ~~circuits other than a storage device~~circuitry regardless of the ~~characteristic of the storage device, all the above problems can be solved~~characteristics of the memory elements.

~~An~~It is therefore an object of the present invention ~~is~~ to provide a nonvolatile memory in which ~~stores~~ information ~~in ferromagnetic substances included~~is stored in terms of the magnetization configuration of a ferromagnet contained in a transistor ~~according to a magnetization state and reads~~and in which the information is sensed using ~~an~~the output

characteristics of the transistor ~~depending~~that depend on the direction of ~~the~~ spin of ~~carriers~~the carrier.

~~According to~~In one ~~viewpoint of~~aspect, the present invention~~, there is provided~~ provides a transistor ~~having~~comprising: a spin injector for injecting spin-polarized hot carriers by a spin-filter effect; and a spin analyzer for selecting the thus injected spin-polarized hot carriers by the spin-filter effect. ~~The~~ Thus, the output characteristics of the transistor can be controlled depending on the spin direction of the spin ~~of the spin~~-polarized hot carriers.

~~Preferably, the~~The spin injector ~~has~~preferably comprises a first ferromagnetic barrier layer, a first nonmagnetic electrode layer joined to one end surface of the first ferromagnetic barrier layer, and a second nonmagnetic electrode layer joined to the other end surface of the first ferromagnetic barrier layer.

~~Preferably, the~~The spin analyzer ~~has~~preferably comprises: a second ferromagnetic barrier layer~~,~~; the second nonmagnetic electrode layer ~~joined to one end surface of the second ferromagnetic barrier layer,~~; and a third nonmagnetic electrode layer joined to the other end surface of the second ferromagnetic barrier layer~~, and shares the~~. The second nonmagnetic electrode layer ~~with~~is joined to one end surface of the second ferromagnetic barrier layer. The second nonmagnetic electrode layer is common to the spin injector~~.~~ and the spin analyzer.

~~Preferably, the~~The first and second ferromagnetic barrier layers ~~include~~preferably comprise an insulating ferromagnetic semiconductor or a ferromagnetic insulator~~, and the~~. The energy band edges of these ferromagnetic barrier layers ~~are constituted by any one of~~is preferably formed by an up-spin band ~~and~~or a down-spin band ~~by the~~due to spin ~~split. Preferably, the~~splitting. The thickness of the second nonmagnetic electrode layer is ~~below~~preferably not greater than the mean free path of the spin- polarized hot carriers ~~of~~in the second nonmagnetic electrode layer.

~~The~~In the spin injector ~~has a large tunnel~~, the tunneling probability ~~to carriers having~~with respect to the carriers with a spin parallel to the spin band ~~constituting~~forming the band edge of the first ferromagnetic barrier layer ~~and a small tunnel probability to carriers having a spin anti-parallel thereto. The carriers having a spin parallel to the spin band constituting~~is large, whereas that with respect to the carriers with an antiparallel spin is small. Thus, carriers with a parallel spin with the spin band forming the band edge of the first ferromagnetic barrier layer can be injected ~~as hot carriers~~ from the first nonmagnetic electrode ~~into~~to the second nonmagnetic electrode layer as hot carriers.

~~The~~On the other hand, the spin analyzer ~~conducts, by~~, due to the spin-splitting at the band edge of the second ferromagnetic barrier layer, ~~the spin~~ allows the spin-polarized hot carriers to be transported to the third nonmagnetic electrode layer when the spin direction of the spin ~~of the spin~~-polarized hot carriers injected into the second nonmagnetic electrode is parallel to the spin direction of the spin ~~of the spin~~ band at the band edge of the second ferromagnetic barrier layer ~~and~~. However, the spin analyzer does not ~~conduct~~allow the spin-polarized hot carriers to be transported to the third ferromagnetic electrode when the spin direction of the spin-polarized hot carriers is ~~anti-parallel to the direction of the spin~~antiparallel to that of the spin band at the band edge of the second ferromagnetic barrier layer.

~~The~~Thus, even under the same bias condition, the output characteristics of the transistor ~~under the same bias depends~~depend on the relative ~~directions of~~ magnetization ~~of the first ferromagnetic barrier layer and the~~configuration of the first ferromagnetic barrier layer and second ferromagnetic barrier layer. ~~When the first ferromagnetic barrier layer and the~~ Specifically, the current transfer ratio or current gain is large when the first ferromagnetic barrier layer and second ferromagnetic barrier layer have parallel magnetization~~, a current transmission factor or a current amplification factor is high. When they have anti parallel magnetization, a current transmission factor or a current amplification factor is low.~~ and it is small when they have antiparallel magnetization.

~~There is provided~~The invention also provides a nonvolatile memory circuit in which ~~stores information according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer and reads the information based on the output characteristic of the transistor depending on the magnetization state. The memory circuit can constitute a memory cell by the transistor alone.~~information can be stored in terms of the relative magnetization configuration of the second ferromagnetic barrier layer and the first ferromagnetic barrier layer, and in which the information can be sensed using the output characteristics of the transistor that depend on the magnetization configuration. In this memory circuit, a memory cell can be configured with a single transistor.

~~According to another aspect of the present invention, there is provided a nonvolatile memory circuit having means storing information according to the directions of magnetization of ferromagnetic substances using a spin transistor including the ferromagnetic substances having an output characteristic depending on the direction of the spin of carriers, and means electrically reading the information stored in the spin transistor from the output characteristic.~~

In another aspect, the invention provides a nonvolatile memory circuit comprising a spin transistor containing a ferromagnet and having output characteristics that depend on the spin direction of the carriers, a means for storing information in terms of the relative magnetization configuration of the ferromagnet, and a means for electrically sensing information stored in the spin transistor using the output characteristics.

~~Preferably, the~~The spin transistor ~~has~~preferably comprises at least one ~~ferromagnetic substance (hereinafter, called~~ferromagnet (to be hereafter referred to as a "free layer") ~~capable of independently controlling the direction of magnetization and at least one ferromagnetic substance (hereinafter, called a "pin layer") not changing the direction of magnetization, and holds, as stored information,~~in which the relative magnetization configuration can be independently controlled, and at least one ferromagnet in which the relative magnetization configuration is not changed (to be hereafter referred to as a "pin layer"). Stored information is retained in the form of a first state in which the ~~direction of magnetization~~relative magnetization configuration of the free layer is the same as ~~the direction of magnetization~~that of the pin layer ~~and~~, or a second state in which ~~the directions of magnetization~~their magnetization configurations are different.

Preferably, the spin transistor ~~has~~comprises: a first electrode structure for injecting spin-polarized carriers~~,~~; a second electrode structure for receiving the spin-polarized carriers~~,~~; and a third electrode structure for controlling the ~~quantity~~amount of the

spin--polarized carriers ~~conducted~~transported from the first electrode structure to the second electrode structure~~, and the~~. The pin layer and the free layer are preferably included in any ~~one~~ of the first to third electrode structures.

~~There is provided a storage~~The invention also provides a memory circuit ~~having a spin transistor arrayed~~comprising: the aforementioned spin transistors arranged in a matrix~~,~~; a ~~word line~~wordline connected to the third electrode structures~~,~~; a first ~~wire grounding~~line connecting the first electrode ~~structure,~~structures to ground; and a ~~bit line~~bitline connected to the second electrode ~~structure.~~structures. A plurality of ~~word lines~~wordlines are extended in the column direction~~. Multiple bit lines~~, and a plurality of bitlines are extended in the direction ~~crossing the same~~ (the row direction)~~.~~ perpendicular to the column direction. The spin transistors ~~is arrayed~~ are disposed near the ~~cross point~~intersections of the ~~word line~~wordlines and ~~the bit line~~bitlines.

~~The~~In the aforementioned memory circuit ~~inverts~~, the magnetization ~~of~~in the free layer ~~by~~can be reversed by a magnetic ~~fields induced by flowing electric currents to a first another wire and a second another wire crossing in the state of being electrically insulated from each other on the spin transistor to change~~field induced by a current caused to flow through a first separate line and a second separate line intersecting one another above the spin transistor in an electrically insulated manner, whereby the relative magnetization ~~state of~~configuration between the free layer and the pin layer ~~for storing (or rewriting) information.~~ can be changed so that information can be stored (or written).

~~In place of the first another wire and the second another wire or any one of the first another wire and the second another wire, the word line and the bit line can be used or any one of the word line and the bit line can be used.~~

It is possible to use the wordline and/or the bitline instead of the first separate line and/or the second separate line.

~~The~~In the aforementioned memory circuit ~~can read~~, information ~~based on~~can be sensed using the output characteristics of the spin transistor when the free layer and the pin layer ~~included~~ in the spin transistor have parallel magnetization.

~~There is provided the~~The memory circuit ~~in which~~may comprise an output terminal ~~is~~ formed ~~at~~on one end of each ~~of the bit lines~~bitline, and a second ~~wire~~line ~~branched~~ing from each ~~of the bit lines~~bitline and connected ~~via a load~~ to a power ~~source is provided.~~ supply via a load.

In this case, the information can be ~~read by~~sensed from an output voltage obtained ~~based on~~from the voltage drop ~~of~~across the load ~~by an electric~~due to a current ~~produced between~~through the first and second electrode structures of the spin transistor, the output voltage depending on the relative magnetization ~~state of~~configuration between the free layer and the pin layer.

Using the ~~above~~aforementioned circuit ~~can provide~~, a high--integration density and high-speed nonvolatile memory circuit ~~with high integration density~~can be provided in which ~~can design an~~the output voltages ~~according to a~~ depending on the magnetization ~~state in~~configuration within the transistor ~~by a~~can be designed via the load and ~~a~~ power ~~source~~supply.

BRIEF DESCRIPTION OF THE DRAWINGS

~~FIGS. 1(A) and 1(B) are diagrams showing~~Fig. 1 shows the structure of a spin ~~-~~filter transistor according to ~~this~~an embodiment~~, in which FIG. 1(A) is~~ of the invention. Fig. 1 (A) shows a schematic cross~~-sectional view and FIG. 1(B) is~~ section. Fig. 1 (B) shows an energy band diagram of a conduction band~~s~~ (or a valence band~~s~~) of the structure shown in ~~FIG. 1(A)~~Fig. 1 (A), together with the ~~directions of the spins of the spin bands of~~spin direction of a spin band in the barrier ~~layers;~~ layer.

~~FIGS. 2(A) and 2(B) are~~Fig. 2 shows an energy band ~~diagrams when applying base ground~~diagram in a case where a common-base bias ~~voltages~~voltage is applied between the emitter (~~a~~ first nonmagnetic electrode layer)~~, the base (a second nonmagnetic electrode layer), and the~~ and collector (~~a~~ third nonmagnetic electrode layer) of the spin ~~filter transistor according to this embodiment, in which FIG. 2(A) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are parallel to each other and FIG. 2(B) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are anti parallel to each other;~~ filter transistor of the present embodiment. Fig. 2 (A) shows a case where the relative magnetization configuration of the first and second ferromagnetic barrier layers is parallel. Fig. 2 (B) shows a case where the relative magnetization configuration of the first and second ferromagnetic barrier layers is antiparallel.

~~FIGS. 3(A) and 3(B) are diagrams showing a static characteristic in the base ground of the spin filter transistor according to this embodiment in which the horizontal axis indicates collector base voltage V_{CB} in the right direction in the drawing~~Fig. 3 shows the static characteristics of the spin-filter transistor of the present embodiment in a common-base configuration. The horizontal axis shows collector-base voltage V_{CB} to the right and emitter~~-~~base voltage V_{EB} ~~into~~ the left ~~direction therein and the~~at the top of the figure. The vertical axis ~~indicates~~shows emitter current I_E, base current I_B, and collector current I_C~~, in which FIG. 3(A) shows a characteristic of the case that the magnetization state~~. Fig. 3 (A) shows the characteristics in a case where the magnetization configuration between the ferromagnetic barrier layers of the emitter and the collector is parallel~~ magnetization and FIG. 3(B) shows a characteristic of the case that it is anti-parallel magnetization;~~ , while Fig. 3 (B) shows the characteristics in the case of antiparallel magnetization.

~~FIG. 4(A) is a diagram showing a structural example of memory cells using spin filter transistors 1 according to this embodiment, FIG. 4(B) is a diagram showing a structural example of a memory circuit, and FIG. 4(C) is a diagram in which the vertical axis indicates collector current I_C, the horizontal axis indicates collector emitter voltage V_{CE}, and an I_C V_{CE} characteristic of spin filter transistors 1 and a load straight line by a load resistance are shown in the same drawing;~~

~~FIG. 5(A) is a diagram schematically showing an example of an output characteristic of a current driven type spin transistor, and FIG. 5(B) is a diagram schematically showing an example of an output characteristic of a voltage driven type spin transistor;~~

~~FIG. 6(A) is a diagram showing a structural example of memory cells using voltage driven type spin transistors according to this embodiment, FIG. 6(B) is a diagram showing a structural example of a memory circuit, and FIG. 6(C) is a diagram in which the~~

~~vertical axis indicates drain current I_D, the horizontal axis indicates drain-source voltage V_{DS}, and an I_D-V_{DS} characteristic of voltage-driven type spin transistors 150 and a load curve by active load are shown in the same drawing;~~

Fig. 4 (A) shows an example of a memory cell utilizing a spin-filter transistor 1 of the present embodiment. Fig. 4 (B) shows an example of a memory circuit. The vertical axis of Fig. 4 (C) shows collector current I_C, and the horizontal axis shows collector-emitter voltage V_{CE}, together with the I_C-V_{CE} characteristics of the spin-filter transistor 1 and a load line due to a load resistor.

Fig. 5 (A) shows an example of the output characteristics of a current-driven spin transistor. Fig. 5 (B) schematically shows an example of the output characteristics of a voltage-driven spin transistor.

Fig. 6 (A) shows an example of a memory cell employing a voltage-driven spin transistor of the present embodiment. Fig. 6 (B) shows an example of a memory circuit. The vertical axis of Fig. 6 (C) shows drain current I_D, and the horizontal axis shows drain-source voltage V_{DS}, the figure also showing the I_D-V_{DS} characteristics of a voltage-driven spin transistor 150 and a load curve due to an active load in the same chart.

~~FIG~~Fig. 7 ~~is~~shows an energy band diagram ~~showing a structural~~of an example of a hot -electron transistor type spin transistor~~;~~.

~~FIG~~Fig. 8 ~~is~~shows an energy band diagram ~~showing a structural~~of an example of a hot -electron transistor type spin transistor ~~using heat release~~employing thermionic emission injection~~;~~.

~~FIG~~Fig. 9 ~~is~~shows an energy band diagram ~~showing a structural~~of an example of a hot -electron transistor type spin transistor ~~using a~~utilizing the spin -filter effect~~;~~.

~~FIG~~Fig. 10 ~~is~~shows an energy band diagram ~~showing a structural~~of an example of a tunnel base transistor type spin transistor~~;~~.

~~FIG. 11 is a cross-sectional view showing a structural example of a MOS transistor type spin transistor;~~

Fig. 11 shows a cross section of a MOS transistor type spin transistor.

~~FIG~~Fig. 12 ~~is~~shows a cross~~-sectional view showing a structural example~~ section of a modulation -doped transistor type spin transistor~~;~~.

~~FIG~~Fig. 13 ~~is~~shows a cross~~-sectional view showing a structural~~ section of an example of a MOS transistor type spin transistor ~~having~~comprising a ferromagnetic semiconductor channel~~;~~.

~~FIG~~Fig. 14 ~~is~~shows a cross~~-sectional view showing a structural~~ section of an example of a spin transistor ~~having a structure in which a gate insulator film and a gate electrode are provided to~~comprising a ferromagnetic source, a ferromagnetic drain, and a nonmagnetic insulating tunnel barrier ~~provided between a ferromagnetic source and a ferromagnetic drain;~~disposed between the source and the drain, wherein a gate insulating film and a gate electrode are formed on the tunnel barrier.

~~FIG. 15 is a cross-sectional view showing a structural example of a spin transistor having a structure in which a gate insulator film and a gate electrode are provided to an insulating ferromagnetic tunnel barrier provided between a ferromagnetic source and~~Fig. 15 shows a cross section of an example of a spin transistor comprising a ferromagnetic source, a ferromagnetic drain or a nonmagnetic drain~~;~~, and an insulating

ferromagnetic tunnel barrier disposed between the source and drain, wherein a gate insulating film and a gate electrode are formed on the tunnel barrier.

~~FIG. 16(A) is a diagram showing a structural example of memory cells having a shared source structure;~~

~~FIG. 16(B) is a diagram showing a cross-sectional structure example of the memory cells having a shared source structure; and~~

Fig. 16 (A) shows an example of a memory cell with a common-source configuration.

Fig. 16 (B) shows a cross section of a memory cell with a common-source configuration.

~~FIG~~Fig. 17 (A) ~~is a diagram showing~~shows the structure of a ~~typical~~conventional MRAM ~~using an MTJ, and FIG. 17(B) is a diagram showing~~utilizing a MTJ. Fig. 17 (B) shows the operating principle of the MTJ.

BEST MODE FOR CARRYING OUT THE INVENTION ~~A~~The transistor according to the present invention ~~has~~comprises a spin injector for injecting spin-polarized hot carriers having ~~the~~a specific spin direction ~~of a specified spin, and a spin analyzer~~, and a spin analyzer for selecting the thus injected spin-polarized hot ~~carriers according to the direction of the spin.~~carries by their spin directions. The spin injector ~~has~~comprises a first ferromagnetic barrier layer ~~having~~with such a thickness ~~permitting a tunnel effect~~allowing for tunneling, such as Fowler-Nordheim ~~tunnel or direct tunnel, a first nonmagnetic electrode layer joined to one end surface of the first ferromagnetic barrier layer, and a second nonmagnetic electrode layer~~tunneling or a direct tunneling; a first nonmagnetic electrode layer joined to one end surface of the first ferromagnetic barrier layer; and a second nonmagnetic electrode layer joined to the other end surface of the first ferromagnetic barrier layer. The spin analyzer ~~has~~ comprises a second ferromagnetic barrier layer~~,~~; a second nonmagnetic electrode layer joined to one end surface of the second ferromagnetic barrier layer~~,~~; and a third nonmagnetic electrode layer joined to the other end surface of the second ferromagnetic barrier layer~~, and shares the second nonmagnetic electrode layer with the spin injector.~~. The second nonmagnetic electrode layer is common to the spin analyzer and the spin injector. The thickness of the second nonmagnetic electrode layer is preferably ~~below~~not greater than the mean free path of the spin-polarized hot carriers ~~of~~in the nonmagnetic electrode layer.

~~The~~When the above-described structure is compared with ~~the structure~~that of a ~~known~~conventional hot electron transistor~~,~~ ~~T~~the first nonmagnetic electrode layer and the first ferromagnetic barrier layer correspond to ~~an~~the emitter and ~~an emitter barrier. The~~the emitter barrier, respectively; the second nonmagnetic electrode layer corresponds to ~~a~~the base~~. The~~; and the second ferromagnetic barrier layer and the third nonmagnetic electrode layer correspond to ~~a collector barrier and a collector~~the collector barrier and the collector, respectively.

The first and second ferromagnetic barrier layers ~~include~~comprise an insulating ferromagnetic semiconductor or a ferromagnetic insulator. The energy bands of these ferromagnetic barrier layers are spin-split by magnetic exchange interaction~~. Only~~, and only an up-spin band or ~~only~~ a down-spin band exists at the band edges ~~by the~~due to

this spin ~~split.~~splitting. The energy width in which only one of the spin bands exists is ~~called~~referred to as a spin -split width.

~~According to the spin~~ The spin-filter effect of the spin injector takes advantage of the following fact. Namely, in the tunneling effect, such as Fowler--Nordheim (FN) tunneling or a direct ~~tunnel produced by applying~~tunneling, in which a voltage is applied to the first ferromagnetic barrier layer via the first nonmagnetic electrode layer and the second nonmagnetic electrode layer ~~to the first ferromagnetic barrier layer, large is the tunnel probability of the carriers having the direction of the spin (when the carriers are electrons, referring to the direction of the spin anti parallel to the magnetization of the first ferromagnetic barrier layer, and when the carriers are holes, referring to the spin parallel to the magnetization of the first ferromagnetic barrier layer) matched with the direction of the spin~~, those of the carriers in the first nonmagnetic electrode layer that have a spin direction corresponding to that of the spin band at the band ~~edge~~end of the first ferromagnetic barrier layer (the spin direction being antiparallel to the magnetization of the first ferromagnetic barrier layer when the carriers are electrons, or parallel to the magnetization of the first ferromagnetic barrier layer when the carriers are hole) have a large tunneling probability, whereas those with a spin direction that does not correspond (the spin direction being parallel to the magnetization of the first ferromagnetic barrier layer ~~of the carriers of the first nonmagnetic electrode layer, and small is the tunnel probability of the carriers having the direction of the spin (when the carriers are electrons, referring to the direction of the spin parallel to the magnetization of the first ferromagnetic barrier layer, and when the carriers are holes, referring to the spin anti parallel to the magnetization of the first ferromagnetic barrier layer) not matched therewith~~when the carriers are electrons, or antiparallel to the first ferromagnetic barrier layer when the carriers are holes) have a small tunneling probability.

~~According to the~~The spin -filter effect of the spin analyzer~~, in~~ takes advantage of the ~~case of~~fact that, when injecting spin--polarized hot carriers from the spin injector into the spin -split band of the second ferromagnetic barrier layer, ~~when the direction of the spin of the injected spin-polarized hot carriers is parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer (the first and second ferromagnetic barrier layers have parallel magnetization), the spin~~ the spin-polarized hot carriers are ~~conducted~~transported through the spin band ~~of~~in the second ferromagnetic layer ~~to~~and arrive at the third nonmagnetic electrode layer~~, and when the direction of the spin of the spin-polarized hot carriers is anti-parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer (the first and second ferromagnetic barrier layers have anti-parallel magnetization), the spin~~ when the spin direction of the injected spin-polarized hot carriers is parallel to that of the spin band at the band edge of the second ferromagnetic barrier layer (where the first and second ferromagnetic barrier layers have parallel magnetization), whereas when the spin direction at the band edge of the second ferromagnetic barrier layer is antiparallel to that of the spin-polarized hot carriers (where the first and second ferromagnetic barrier layers have antiparallel magnetization), the spin-polarized hot carriers cannot be ~~conducted~~transported through the second ferromagnetic barrier layer.

~~According to the above structure~~In this arrangement, the carriers in the first

nonmagnetic electrode layer ~~having~~with the spin direction ~~of the spin~~ parallel to ~~the direction of the spin~~that of the spin band at the band edge of the first ferromagnetic barrier ~~layer~~ are injected as spin-polarized hot carriers into the second nonmagnetic electrode layer by ~~the tunnel effect~~tunneling, such as Fowler-Nordheim tunneling or a direct ~~tunnel. At this time, the above~~tunneling. The transistor is biased ~~so~~such that the energy of the ~~injected spin~~ thus injected spin-polarized hot carriers is larger than the energy ~~at~~of the spin ~~band edge at the~~ band edge of the second ferromagnetic barrier layer and ~~is~~ smaller than the energy ~~in~~of the spin band edge to which the spin -split width ~~is applied to the spin band edge. The~~has been added. Since the thickness of the second nonmagnetic electrode layer is ~~below~~not greater than the mean free path of the spin-polarized hot carriers in the second nonmagnetic electrode layer., ~~T~~the injected spin-polarized hot carriers ~~reach~~arrive at the second ferromagnetic barrier layer without losing energy. ~~The~~ In addition, the energy of the spin-polarized hot carriers is larger than ~~the energy~~that of the spin band edge at the band edge of the second ferromagnetic barrier layer and is smaller than the energy ~~in~~of the spin band edge to which the spin ~~split width is added to the spin band edge. When the direction of the spin of the injected spin~~ -split width has been added. Therefore, when the spin direction of the injected spin-polarized hot carriers is parallel to the ~~direction of the spin~~spin direction of the spin band at the band edge of the second ferromagnetic barrier layer, the spin-polarized hot carriers are ~~conducted through~~transported within the spin band by an electric field produced in the second ferromagnetic barrier layer, ~~are carried~~and transported to the third nonmagnetic electrode layer, ~~and become an electric~~producing a current ~~flowing~~that flows between the third nonmagnetic electrode layer and the first nonmagnetic electrode layer.

~~When the direction of the spin~~On the other hand, when the spin direction of the injected spin-polarized hot carriers is ~~anti-parallel~~antiparallel to the ~~direction of the spin~~spin direction of the spin band at the band edge of the second ferromagnetic barrier layer, the spin-polarized hot carriers are scattered (or ~~backscattered) at~~reflected) by the ~~interface of~~ boundary between the second nonmagnetic electrode layer and the second ferromagnetic barrier layer, ~~and become an electric~~producing a current ~~flowing~~that flows between the second nonmagnetic electrode layer and the first nonmagnetic electrode layer.

~~Depending~~Thus, depending on whether the relative ~~directions of~~ magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer, namely, whether they are parallel or ~~anti-parallel~~antiparallel, the ~~electric~~ current ~~flowing~~that flows in the first ferromagnetic barrier layer can be switched to ~~the electric~~a current ~~flowing via the second ferromagnetic barrier layer~~that flows between the third nonmagnetic electrode layer and the first nonmagnetic electrode layer ~~or the electric current flowing via the same~~via the second ferromagnetic barrier layer, or a current that flows between the second nonmagnetic electrode layer and the first nonmagnetic electrode layer. ~~The electric current flowing via~~ Namely, the current through the second ferromagnetic barrier layer can be controlled ~~according to~~by the relative ~~directions of~~ magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer. ~~This corresponds to control of a collector current by a base current, as~~ When compared with the operation of ~~a~~ known common-base or common-emitter hot electron ~~transistor and bipolar transistor of a base ground or an emitter ground. The transistor~~

~~according to this embodiment can control the current amplification factor~~transistors or bipolar transistors, the above-described operation of the present embodiment corresponds to controlling the collector current by means of the base current. However, in the transistor of the present embodiment, the factor of amplification of ~~a~~the collector current by ~~a~~the base current ~~according to~~can be controlled by the relative ~~directions of~~ magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer. ~~The~~ Thus, the transistor ~~according to this~~of the present embodiment is ~~a transistor~~ capable of controlling the current ~~amplification factor and can control the collector current according to the relative directions of~~gain, whereby collector current can be controlled not only by the base current (or the bias voltage between the first and second nonmagnetic electrodes), but also by the relative magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer ~~as well as to the base current (or a bias voltage between the first and second nonmagnetic electrodes).~~ .

~~The coercivity of~~Furthermore, when the coercive forces of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer ~~is changed or one of the magnetization directions is fixed. A magnetic field having a suitable strength in which any one of the directions of magnetization~~are varied, or when the relative magnetization configuration of one of them is fixed, the relative magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer ~~is inverted is applied to arbitrarily change the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer to parallel or anti-parallel. In other words~~can be changed to be parallel or antiparallel as desired by applying a magnetic field of an appropriate intensity such that the relative magnetization configuration of either the first ferromagnetic barrier layer or the second ferromagnetic barrier layer is reversed. Namely, information can be stored in the transistor.

~~A~~Thus, a memory cell can be ~~const~~fit~~gu~~red ~~using~~ with the above-described transistor. An example of a nonvolatile memory ~~using~~utilizing the transistor ~~according to this embodiment will be described below. The second nonmagnetic electrode layer of the transistor according to this~~of the present embodiment will be hereafter described. The second nonmagnetic electrode layer of the transistor of the embodiment is connected to a word~~line line.~~, and ~~T~~the third nonmagnetic electrode layer of the transistor is connected to a ~~bit line. The bit line~~bitline. The bitline is connected ~~via a load to a power source to ground the first nonmagnetic electrode layer of the transistor. According to this structure, a specified word line is selected to apply~~to a power supply via a load, and the first nonmagnetic electrode layer of the transistor is grounded. In this arrangement, when a specific wordline is selected and a bias is applied to the second nonmagnetic electrode layer. ~~A specified bit line is selected to detect an~~, the output voltage (~~a~~voltage ~~produced~~that appears at the ~~edge of the~~ third nonmagnetic electrode). ~~The output voltage is changed according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer of the transistor. When the relative directions of magnetization~~ detected by selecting a specific bitline is seen to vary depending on the relative magnetization configuration of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer of the transistor. Namely, when the relative magnetization configuration are parallel, the output voltage ~~is smaller. When the relative directions of~~

~~magnetization are anti-parallel, the output voltage is larger. Stored~~becomes smaller, while when the relative magnetization configuration is antiparallel, the output voltage becomes larger. Thus, the information that is stored can be ~~read depending on~~sensed on the basis of the magnitude of the output voltage.

In the above-described nonvolatile memory, the transistor ~~according to this~~of the present embodiment is used as ~~an~~ a common-emitter ~~ground~~ transistor, ~~the~~a power ~~source and~~supply and a load are ~~added~~provided to the collector, and the collector voltage is ~~an output voltage. An output voltage when the first~~obtained as the output voltage. Thus, using peripheral circuitry such as the power supply and load, desired output voltage values can be obtained when the first ferromagnetic barrier layer and second ferromagnetic barrier layers have parallel magnetization ~~by the peripheral circuits as a source voltage and load and an output voltage~~or when they have ~~anti-parallel~~antiparallel magnetization ~~can be designed to desired values. Using~~. Accordingly, the above-described nonvolatile memory can ~~solve the~~overcome the aforementioned problems of the MRAM based on MTJ, the problems being that the tunnel resistance ~~is small and the output voltage is small in the MRAM using the MTJ~~as well as output voltages are small, that the TMR ratio is so small ~~and stored~~that the information that is stored is hard to ~~identify~~be distinguished, and that the ratio of ~~the~~ output voltages ~~is smaller by~~decreases due to the applied bias.

~~The structure~~In the following, the configuration and operation of the above-described transistor ~~will be~~is described ~~below~~ in greater detail with reference made to the drawings. ~~To easily understand the following description, the~~ The transistor ~~according to this~~of the present embodiment ~~is called a spin~~ will be hereafter referred to as a "spin-filter transistor" for facilitating the understanding of the description of the invention.

~~FIGS. 1(A) and 1(B) are diagrams showing the structure~~Fig. 1 shows the configuration of a spin -filter transistor according to ~~this~~the present embodiment~~, in which FIG. 1(A) is~~. Fig. 1 (A) shows a schematic cross~~-sectional view and FIG. 1(B) is~~ section. Fig. 1 (B) shows an energy band ~~diagram of~~of the conduction bands (or the valence ~~bands) of the structure shown in FIG. 1(A) with the directions of the spins of the spin bands of barrier layers.~~band) of the configuration shown in Fig. 1 (A), also showing the spin direction of the spin band in the barrier layer. When the carriers are holes, the direction of ~~the spin~~magnetization at the band edge ~~is matched with the direction of magnetization. When~~corresponds to the spin direction; when the carriers are electrons, the ~~direction of the spin at the band edge is opposite the direction of magnetization.~~ relative magnetization configuration is opposite to that of the spin direction of the band edge.

A spin -filter transistor 1 according to ~~this~~the present embodiment ~~has~~comprises a spin injector 5 ~~having~~comprising: a first ferromagnetic barrier layer ~~2,~~2; a first nonmagnetic electrode layer 3 joined to one end surface of the first ferromagnetic barrier layer ~~2,~~2; and a second nonmagnetic electrode layer 4 joined to the other end surface of the first ferromagnetic barrier layer ~~2; and~~2. The spin-filter transistor 1 also comprises a spin analyzer 8 ~~having~~comprising: a second ferromagnetic barrier layer ~~6, the~~6; a second nonmagnetic electrode layer 4 joined to one end surface of the second ferromagnetic barrier layer ~~6, and the~~6; and a third nonmagnetic electrode layer 7 joined to the other end surface of the second ferromagnetic barrier layer 6. As ~~is apparent~~will be seen from ~~FIG~~Fig. 1 (A), the spin injector 5 and the spin analyzer 8 share the second nonmagnetic electrode layer 4.

~~As the~~The first, second, and third nonmagnetic electrode layers 3, 44, and ~~7,~~7 may be formed by a nonmagnetic metal, an n-type nonmagnetic semiconductor, or a p-type nonmagnetic semiconductor~~ can be used. Preferably, the~~. The thickness of the second nonmagnetic electrode layer 4 is ~~below~~preferably not greater than the mean free path ~~in~~within the nonmagnetic electrode layer 4 of the spin-polarized hot carriers injected from the spin injector.~~ The~~ By making the base width ~~is~~ shorter than the mean free path~~ to allow a,~~ the current ~~transmission factor to be~~transfer ratio can be made 0.5 or ~~above. The~~greater, so that current amplification ~~function can be obtained.~~ can be achieved.

~~As the~~The first and second ferromagnetic barrier layers 2 and ~~6,~~6 may comprise an insulating ferromagnetic semiconductor or a ferromagnetic insulator~~ can be used.~~. The energy band of the ferromagnetic barrier layer is spin -split by magnetic exchange interaction~~. An energy region in which~~, such that an energy region is created at the band edge where only an up- spin or ~~only~~ a down- spin exists~~ can be formed at the band edge. The spin~~. Such a spin-polarized band is ~~called~~referred to as a spin band~~. The energy region width is called a spin~~, and this energy region band is referred to as a spin-split width Δ.

As shown in ~~FIG~~Fig. 1 (B), the solid lines ~~indicated by the arrows ↑ to~~with an arrow ↑ on the ferromagnetic barrier layers 2 and 6 ~~denote~~indicate the edge of the band ~~edges in which~~where an up spin can exist, ~~that is,~~namely, an up -spin band edges 9. The solid lines ~~indicated by the arrows ↓ thereto denote~~with an arrow ↓ indicate the edge of the band ~~edges in which~~where a down spin can exist, ~~that is~~namely, a down -spin band edges 10. The ~~portion~~region between the up -spin band edge 9 and the down -spin band edge 10 in ~~FIG~~Fig. 1 (B) is a region ~~in which~~where only ~~the~~an up spin can exist. A region ~~having an energy~~with a higher energy than that of the down -spin band edge 10 is a region ~~in which~~where both ~~the~~ up spin and ~~the~~ down spin can exist.~~ FIG~~ While Fig. 1 (B) shows ~~the~~a case ~~that~~where the spin band of ~~the~~ up spin is lower than the spin band of ~~the~~ down spin~~.~~, ~~T~~the ~~reverse~~ opposite state is also possible.

The first ferromagnetic barrier layer 2 has a thickness ~~in which~~such that the carriers can be transmitted from the first nonmagnetic electrode layer 4 to the second nonmagnetic electrode layer 4 by ~~the tunnel effect~~tunneling, such as Fowler~~-Nordheim tunnel (hereinafter, called an FN tunnel~~-Nordheim tunneling (to be hereafter referred to as "FN tunneling") or a direct ~~tunnel by~~tunneling, in response to the application of a voltage ~~applied~~ to the first nonmagnetic electrode layer 3 and to the second nonmagnetic electrode layer 4.~~ The~~ A direct tunneling refers to ~~a~~the phenomenon in which the carriers ~~are~~ directly ~~transmitted~~pass through a thin potential barrier. The FN tunneling refers to ~~a~~the phenomenon in which ~~a~~the tunneling current ~~by the~~due to a direct tunneling can be ~~neglected~~ignored up to a certain applied voltage and in which the carriers ~~are tunneled~~tunnel through ~~a~~the triangular potential ~~in~~at the ~~upper portion~~top of a potential barrier produced by ~~applying~~the application of a voltage ~~above~~exceeding a certain value.

~~A~~The voltage applied to the first nonmagnetic electrode layer 3 and the second nonmagnetic electrode layer 4 may be in ~~a~~the voltage range used in ~~a typical~~the conventional memory circuit, ~~e.g., of~~such as on the order of ~~some hundreds of~~several hundred mV to several ~~V~~volts. The ~~thickness of the~~ second ferromagnetic barrier layer 6

~~must be a thickness so that thermal release~~needs to be sufficiently thick that there is no thermionic emission of the carriers ~~and an electric~~or a current ~~by the~~due to tunneling (the so-called leak current) ~~do not occur~~ from the second nonmagnetic electrode layer 4 to the third nonmagnetic electrode layer 7.

The nonmagnetic electrode layers 3, ~~4 and~~4, 7 and the ferromagnetic electrode layers 2 and 6 form the energy band structures shown in ~~FIG~~Fig. 1 (B). Solid lines 11 ~~of~~in the nonmagnetic electrode layer ~~portions in FIG~~Fig. 1 (B) ~~show~~indicate the Fermi energy of ~~a~~the metal, the Fermi energy of an n-type (p-type) semiconductor, or the energy ~~of~~at the bottoms of the conduction bands (at the tops of the valence bands). The lower energy barriers ~~of~~ in the ferromagnetic barrier layers 2 and 6 corresponding to the solid lines 11 ~~of~~at the nonmagnetic electrode layer ~~portions are~~is indicated by $\phi_C\varphi_C$, and the spin -split width~~s are~~ is indicated by ~~Δ. The~~Δ. Although the ferromagnetic barrier layers 2 and 6 may have different ϕ_C ~~and Δ. The case that~~values of φ_C and Δ, the following description concerns a case where the ferromagnetic barrier layers 2 and 6 have the same $\phi_C$values of φ_C and ~~Δ will be shown below. When~~Δ.

In the case where the carriers are electrons, a nonmagnetic metal or an n-type semiconductor is used ~~as~~for the nonmagnetic electrode layers 3, 44, and ~~7~~7, and an insulating ferromagnetic semiconductor or a ferromagnetic insulator is used ~~as~~for the ferromagnetic barrier layers 2 and 6. In this case, the up -spin band edges 9 and the down ~~spin band edges 10~~-spin band edge 10 are produced by the spin splitting of the bottom of the conduction band of the ferromagnetic barrier layers 2 and ~~6 are those in which the bottoms of the conduction bands are spin split. When~~6. In the case where the carriers are holes, a p-type semiconductor is used ~~as~~for the nonmagnetic electrode layers 3, ~~4 and 7~~4, 7, and an insulating ferromagnetic semiconductor or a ferromagnetic insulator is used ~~as~~for the ferromagnetic barrier layers 2 and 6. In this case, the up -spin band edges 9 and the down -spin band edges 10 of the ferromagnetic barrier layers 2 and 6 are ~~those in which the tops~~produced by the spin splitting of the top of the valence ~~bands are spin split~~band.

~~The~~Hereafter, the operating principle of the above-described spin -filter transistor ~~will be~~is described in detail. In the following description, ~~for simplifying the description, the notation of a~~the notational system for the hot electron transistor ~~is used together. The~~will also be used for simplicity's sake. Specifically, the first nonmagnetic electrode layer 3 and the first ferromagnetic barrier layer 2 ~~are called~~will be referred to as an emitter ~~21.~~21, ~~T~~the second nonmagnetic electrode layer 4 ~~is called~~will be referred to as a base ~~22.~~22, ~~T~~the second ferromagnetic barrier layer 6 and the third nonmagnetic electrode layer 7 ~~are called~~will be referred to as a collector ~~23.~~23, ~~T~~the first nonmagnetic electrode layer 3 ~~is called the~~will be referred to as an emitter electrode ~~3. The~~3, and the third nonmagnetic electrode layer 7 ~~is called the~~will be referred to as a collector electrode 7. ~~An example of the case that~~ The following also concerns the case where the carriers are electrons ~~will be described (when~~as an example (the case where the carriers are holes~~, the~~ will not be described because such a case is substantially the same in terms of operating principle ~~is essentially the same and the description is omitted~~).

~~FIGS~~Fig. 2~~(A) and 2(B) are~~ shows energy band diagrams ~~when applying base ground~~in a case where a common-base bias ~~voltages~~voltage is applied between the emitter,

~~the~~ base, and ~~the~~ collector of the spin -filter transistor ~~according to this embodiment, in which FIG. 2(A) shows the case that the directions of~~of the present embodiment. Fig. 2 (A) shows a case where the magnetization configurations of the first and second ferromagnetic barrier layers are parallel to each other ~~and FIG. 2(B) shows the case that the directions of,~~ and Fig. 2 (B) shows a case where the magnetization configurations of the first and second ferromagnetic barrier layers are ~~anti-parallel~~antiparallel to each other ~~and corresponds to FIG. 2(A). Bias~~, corresponding to Fig. 2 (A). A bias voltage V_{EB} is applied ~~between the~~across emitter 21 and ~~the~~ base ~~22. Bias~~22, and a bias voltage V_{CB} is applied ~~between the~~across base 22 and ~~the~~ collector 23. The magnitude of ~~the~~ V_{EB} is set ~~to satisfy~~such that the relationship ~~of (ϕ_C (Φ_C < qV_{EB} < $\phi_C\Phi_C$ +Δ).~~ Δ) is satisfied, where q is ~~a~~the elementary charge ~~quantum~~.

The emitter 21 ~~serves~~functions as a spin injector for injecting spin-polarized hot electrons ~~into the~~to base 22. ~~When the bias voltage V_{EB} tunnel passes~~ Thus, when causing the carriers ~~from the emitter electrode 3~~ to pass through the first ferromagnetic barrier layer ~~2,~~2 from the emitter electrode 3 by tunneling using the bias voltage V_{EB}, since the conduction band of the first ferromagnetic barrier layer 2 is spin ~~split and the barrier heights felt by an up spin electron 24 and a down spin electron 25 existing~~-split, the barrier height for the up-spin electrode 24 and that for the down-spin electrode 25 in the emitter electrode 3 are different. ~~In FIG. 2~~

Namely, in Fig. 2 (A), the barrier height ~~felt by the up spin electron 24 is an energy to the up~~ for the up-spin electrode 24 corresponds to the energy up to an up-spin band edge 9 of the first ferromagnetic barrier layer 2, ~~that is, ϕ_C,~~ or Φ_C. The barrier height ~~felt by the down spin electron 25 is an energy to the down~~ for the down-spin electrode 25 corresponds to the energy up to a down-spin band edge 10 of the first ferromagnetic barrier layer 2, ~~that is, ϕ_C + Δ. Control of~~for Φ_C+Δ. Thus, by controlling the base ~~emitter voltage can selectively tunnel inject, as a hot electron, the electron having a spin having a lower felt barrier height, in this case, the electron 24 having an up spin into the base 22 (this phenomenon is~~-emitter voltage, electrons with a spin for which the barrier height is lower, namely, an up spin, which correspond to electrons 24 in the illustrated example, can be selectively tunnel-injected to the base 22 (in a phenomenon called ~~the~~ "spin -filter effect~~)~~") as hot electrons.

The collector 23 of the spin -filter transistor ~~serves~~functions as a spin analyzer for selecting the direction of the spin-polarized hot electrons injected into the base 22. ~~A spin polarized hot electron 26 which becomes hot~~ Specifically, the spin-polarized electrons 26 that have been rendered into hot electrons by the bias voltage V_{EB} and ~~is~~-injected into the base ~~22, since the width of the base 22 is set below the mean free path of the spin polarized hot electron 26, can ballistically~~22 can arrive at the ~~interface of the~~boundary between base 22 and ~~the~~ collector 23 without losing energy~~.~~, or "ballistically," because the width of base 22 is set to be not greater than the mean free path of the spin-polarized hot electrons 26. In the second ferromagnetic barrier layer 6 of ~~the~~ collector 23, there is also produced two barriers ~~having~~with different barrier heights ~~occur by~~due to the spin splitting of the conduction ~~bands.~~band. As shown in ~~FIG~~Fig. 2 (A), when the ~~directions of~~ magnetization configurations of the first and second ferromagnetic barrier

layers 2 and 6 are parallel to each other, because the up -spin band edge 9 of the second ferromagnetic barrier layer 6 having a spin parallel to that of the spin ~~-polarized hot electron 26 has an energy lower than that of the spin-polarized hot electron 26. The spin-polarized hot electron 26 is conducted to cross over~~-polarized hot electrons 26 is lower than the energy of the spin-polarized hot electrons 26, the spin-polarized hot electrons 26 are transported to the collector electrode 7 across the second ferromagnetic barrier layer ~~6 to the collector electrode 7 to be~~6, thereby producing a collector current I_C.

~~As shown in FIG. 2(B)~~On the other hand, when the ~~directions of~~ magnetization configurations of the first and second ferromagnetic barrier layers 2 and 6 are ~~anti-parallel~~antiparallel to each other, ~~a~~as shown in Fig. 2 (B), spin--polarized hot electrons 27 ~~having a~~with down spin ~~is~~are injected ~~into the~~to a base 22. ~~The~~ In this case, however, because the down -spin band edge 10 of the second ferromagnetic barrier layer 6 ~~having a~~with down spin ~~has an energy~~is higher than ~~that~~the energy of the spin--polarized hot electrons ~~27.~~ 27, ~~T~~the spin--polarized hot electrons 27 cannot be ~~conducted~~transported through the conduction band of the second ferromagnetic barrier layer ~~6 and is subject~~6. Instead, they lose energy as they are subjected to spin--dependent scattering (or ~~backscattering~~reflection) at the ~~interface of the~~boundary between base 22 and ~~the~~ collector ~~23 to lose energy to become~~23, resulting in a flow of base current I_B.

~~The current transmission factor of an electric current flowing~~Thus, the current transfer ratio of the current that flows from the emitter to the collector ~~is largely different~~greatly differs depending on the relative ~~directions of~~ magnetization configuration of the first ferromagnetic barrier layer 2 of ~~the~~ emitter 22 and the second ferromagnetic barrier layer 6 of ~~the~~ collector 23. In other words, the current ~~amplification factor~~gain of ~~the~~ collector current ~~by the~~due to base current ~~is largely different~~greatly differs.

~~FIGS. 3(A) and 3(B) are diagrams showing a static characteristic in the base ground~~Fig. 3 shows the static characteristics of the spin -filter transistor ~~according to this~~of the present embodiment in ~~which the~~a common-base configuration. The horizontal axis ~~indicates~~shows collector--base voltage V_{CB} in the upper-right ~~direction in the drawing~~portion and emitter--base voltage V_{EB} ~~into~~ the left ~~direction therein and the~~. The vertical axis ~~indicates~~shows emitter current I_E, the base current I_B, and collector current I_C; ~~in which FIG. 3(A) shows a static characteristic of the case that the directions of~~. Fig. 3 (A) shows the static characteristics in a case where the magnetization configurations of the ferromagnetic barrier layers of the emitter and the collector are parallel ~~and FIG. 3(B) shows a static characteristic of the case that they are anti-parallel. In FIGS~~. Fig. 3 (B) shows the static characteristics when the magnetization configurations are antiparallel. In both Fig. 3 (A) and ~~3~~(B), ~~α is a current transmission factor, β is a current amplification factor~~α indicates the current transfer ratio, β indicates the current gain, and the subscripts $\uparrow\uparrow$ and $\downarrow\uparrow$ indicate the ~~case that the~~parallel and antiparallel relative ~~directions of~~ magnetization configuration, respectively, of the ferromagnetic barrier layers of the emitter and ~~the~~ collector ~~are parallel and the case that they are anti-parallel.~~.

As shown in ~~FIG~~Fig. 3 (A), when the ~~directions of~~ magnetization configurations of the emitter and the collector are parallel, most of the emitter current I_E can ~~be~~serve as the collector current I_C. As shown in ~~FIG~~Fig. 3 (B), when the ~~directions of~~

magnetization are anti parallelmagnetization configurations are antiparallel, most of the emitter current I_E can beserve as the base current I_B. Like a As in the known hot electron transistors or bipolar transistor, the transistor according to this embodiment can controltransistors, the collector current I_C can be controlled by the base current I_B. It can control the current amplification factor according to in the transistor of the present embodiment. In addition, the current gain can be controlled by the relative directions of magnetization configuration of the first and second ferromagnetic barrier layers.

As theThe ferromagnetic barrier layer of the spin -filter transistor according to thisof the present embodiment, may comprise a ferromagnetic semiconductor, such as EuS, EuSe, and EuO can be used. Aor EuO, for example. It may also comprise a ferromagnetic insulator, such as $R_3Fe_5O_{12}$ (where R expressesis a rare--earth element) can be also used. As a. The nonmagnetic electrode layer, a may comprise any material as long as it is nonmagnetic substance may be used. For instance, a metal. Examples include metals, such as Al orand Au, or aand nonmagnetic semiconductorsemiconductors, such as Si or GaAs which is impurityand GaAS, that have been doped with a high density may be used. When EuS is used as aconcentration of impurity. When, for example, the ferromagnetic barrier layer and Al is used as acomprises EuS and the nonmagnetic electrode layer comprises Al, the barrier height $\hat{\Theta}_C = \Phi_C$ is 1.4eV and the spin -split width $\Delta = \Delta$ is 0.36eV. The spin -filter transistor according to thisof the present embodiment can be manufactured using the above materialproduced by a known method, such as molecular beam epitaxial growth methodepitaxy, vacuum deposition method andevaporation, or sputtering method, using the above-described materials.

AIn the following, a nonvolatile memory usingcomprising the spin -filter transistor of the present invention as a memory cell will be described.

FIG. 4(A) is a diagram showing a structuralFig. 4 (A) shows an example of a memory cell using theemploying a spin -filter transistor 1 according to thisof the present embodiment. In the memory cell shown in FIGFig. 4 (A), a number of spin -filter transistors are arranged in a matrix, with the emitter terminals E is grounded to connectand the collector terminals C and base terminal B to read bit line BL and read word line WL. A rewrite word line and a rewrite bit line are arranged to cross each other on the base terminals B connected to a bitline BL for sensing and a wordline WL for sensing, respectively. A wordline for writing intersects a bitline for writing above the spin -filter transistors in such theat state of being these lines are electrically insulated from other wires. As the rewrite word line and the rewrite bit line, the read bit line BL and the read word line WL may be used. FIG. 4(A) is a diagram showing a cell structure of this case. In FIG The wordline for writing and the bitline for writing may be combined with the aforementioned bitline BL for sensing and wordline WL for sensing, as shown in Fig. 4 (A). In the case of Fig. 4 (A), thea memory cell can be constitutedformed by thea single spin filter transistor alone and can have a very simplified structure for wiring. A-filter transistor, and also a simple wiring arrangement can be adopted. Thus, the present memory cell arrangement makes it possible to easily configure a layout suitable for high -density integration can be easily constituted. The same cell structure is used in FIG. 4(B). The example shown in Fig. 4 (B) also adopts a similar cell arrangement.

~~A~~With reference to Fig. 4(B), a memory circuit according to ~~this~~the present embodiment will be described ~~with reference to FIG. 4(B)~~. In a memory circuit 41 ~~according to this~~of the present embodiment, ~~the~~a second nonmagnetic electrode ~~4 as~~4, which is the base of the spin -filter transistor 1 (~~FIG~~Fig. 1), is connected to a ~~word line 42, the~~wordline 42; a third nonmagnetic electrode ~~7 as~~7, which is the collector electrode of the spin -filter transistor ~~1~~1, is connected to a ~~bit line 43,~~bitline 43; the ~~bit line~~bitline 43 is connected ~~via a load (R_L) 44~~ to a power ~~source~~supply (V_{CC}) ~~45,~~45 via a load (R_L) 44; and ~~the~~a first nonmagnetic electrode ~~3 as~~3, which is the emitter electrode of the spin -filter transistor ~~1 is grounded. A~~1, is connected to ground. Although a pure resistance is used as the load~~. An~~ in the illustrated example, an active load ~~by the~~consisting of a transistor may be used.

~~To read stored~~When sensing information ~~of~~stored in a specified~~c~~ memory cell, ~~the specified word line~~a specific wordline 42 is selected ~~to apply~~and a bias ~~between~~is applied across the emitter ~~and the base, the source~~-base junction, and a power supply voltage V_{CC} ~~of~~from the power ~~source~~supply 45 is applied to the bitline 43 via the load resistance ~~44 to the bit line 43,~~44. Then, the stored information is ~~read according to~~sensed using the magnitude of an output voltage V_O ~~appearing on~~that appears at the ~~bit line~~bitline 43. ~~In FIG. 4(C), the~~ The vertical axis ~~indicates~~of Fig. 4 (C) shows collector current I_C~~,~~. ~~t~~The horizontal axis ~~indicates~~shows collector~~-~~-emitter voltage V_{CE}~~, and an I_C-V_{CE} characteristic~~. The graph thus shows the I_C-V_{CE} characteristics of the spin -filter transistor and a load ~~straight~~ line 46 ~~by~~of the load resistance 44 ~~are shown~~ in the same ~~drawing~~chart.

The output voltage V_O is determined ~~from~~by the ~~crossing point~~intersection of these characteristics. ~~Output voltages in which~~ Specifically, the output signals in the ~~mutual~~cases where the magnetization ~~states of~~configuration between the first and second ferromagnetic barrier layers 2 and 6 ~~are~~is parallel and ~~anti-parallel are~~ ~~$V_{O\uparrow\uparrow}$~~antiparallel would be $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow\downarrow\uparrow}$, as shown in ~~FIG~~Fig. 4 (C). The absolute values of ~~the~~ ~~$V_{O\uparrow\uparrow\uparrow\uparrow}$~~ and $V_{O\downarrow\uparrow\downarrow\uparrow}$ and the ratio of ~~the~~ ~~$V_{O\uparrow\uparrow\uparrow\uparrow}$~~ and $V_{O\downarrow\uparrow\downarrow\uparrow}$ can be optimized by ~~the~~means of circuit parameters (R_L and V_{CC}). ~~The~~ Thus, using the nonvolatile memory device ~~according to this~~of the present embodiment ~~can obtain~~, output signals ~~having a necessary magnitude and the~~of required magnitudes and a required ratio of output signals can be obtained without adjusting the structure of the ~~device itself unlike the~~elements themselves, as in a MTJ.

The spin -filter effect ~~used in~~utilized by the transistor ~~according to this embodiment is an effect using the spin split of the bands of the ferromagnetic substances and has a spin selectivity higher~~of the present embodiment is provided by the spin band splitting of the ferromagnet, such that a higher spin selectivity can be obtained than ~~that of~~is possible with the TMR effect of ~~the~~MTJ. When the base width is set ~~below~~to be no more than the mean free path of the spin~~-~~-polarized hot carriers ~~and~~, the current transfer ratio α (defined as being equal to I_C/I_E) can be 0.5 or more when the relative magnetization ~~state~~configuration between the first and second ferromagnetic barrier layers is ~~parallel magnetization, the current transmission factor α (defined by = I_C / I_E) can be 0.5 or above. When it is anti~~-parallel. However, when the relative magnetization configuration is antiparallel, the current ~~transmission factor is very~~transfer ratio is extremely small. ~~The~~

Thus, the change in the current ~~transmission factor in the case of~~transfer ratio between parallel magnetization and ~~anti-parallel~~antiparallel magnetization is ~~further~~even more amplified~~, seen from the~~ in terms of current ~~amplification factor β~~gain β (defined ~~by =~~as being equal to I_E / I_B~~). The above peripheral circuits optimize~~I_B). By optimizing the output signal using the above-described peripheral circuitry with reference to the output characteristics of the spin -filter transistor ~~which is largely different in~~that vary greatly depending on the magnetization ~~state. The~~configuration, output signals of desired absolute values ~~of output signals~~ and their desired ratio ~~of output signals~~ can be easily obtained.

~~A~~Hereafter a nonvolatile memory circuit ~~using the transistor having an output characteristic depending~~utilizing a transistor (to be hereafter referred to as a "spin transistor") with output characteristics that depend on the spin direction of the ~~spin of~~ carriers ~~(hereinafter, called a "spin transistor") will be~~is described.

The memory circuit ~~according to~~of the present invention relates to a nonvolatile memory circuit ~~using the~~utilizing a spin transistor. ~~The~~ A spin transistor includes ~~ferromagnetic substances~~a ferromagnet such as a ferromagnetic metal ~~and~~or a ferromagnetic semiconductor ~~and controls the~~. The output characteristics are changed by controlling the spin direction of the ~~spin of~~ carriers ~~according to~~depending on the magnetization ~~state to change the output characteristic.~~configuration of the ferromagnet. Information is stored ~~based on the magnetization state of the ferromagnetic substances in the spin transistor. The output characteristic of the transistor reflecting the magnetization state in the spin transistor is used to read the information. A one~~ in terms of the magnetization configuration of the ferromagnet inside the spin transistor, and the stored information is sensed using the output characteristics of the transistor that reflect the magnetization configuration inside the spin transistor. Using the spin transistor, a 1-bit nonvolatile memory cell can be ~~constituted by one~~configured with a single spin transistor. ~~The values~~ Furthermore, the value of the output ~~signals~~signal corresponding to the stored information can be optimized by ~~the~~ peripheral circuitsry connected to the memory cell.

~~In greater detail~~Specifically, the spin transistor ~~has~~comprises at least one ~~ferromagnetic~~each of a ferromagnet layer (free layer) capable of independently controlling the ~~direction of~~relative magnetization ~~by~~configuration using a magnetic field ~~and at least one ferromagnetic~~or the like, and a ferromagnet layer (pin layer) ~~in which the direction of magnetization is fixed~~with a fixed relative magnetization configuration or having a larger coercivity ~~larger~~ than that of the free layer ~~and is a transistor capable of controlling the output characteristic~~. The output characteristics of the transistor ~~according to~~can be controlled by the relative ~~directions of~~ magnetization configuration of the free layer and the pin layer even under the same bias. ~~The direction of~~ condition. By changing the relative magnetization configuration of the free layer ~~is changed by~~using a magnetic field. ~~The relative magnetization states~~, for example, the relative magnetization configuration of the free layer and the pin layer can be ~~two states of parallel magnetization and anti-parallel magnetization. The two magnetization states correspond to~~rendered into two configurations, namely, parallel or antiparallel. These two magnetization configurations are associated with binary stored information.

~~The~~In the spin transistor ~~can obtain the output characteristic according to the~~

~~magnetization state in the transistor,~~ based on a conductive~~on~~ phenomenon ~~changed~~that varies depending on the spin direction of the ~~spin of carriers~~carrier, such as spin-dependent scattering, tunneling magnetoresistance effect, ~~and~~or spin -filter effect~~.~~, output characteristics corresponding to the internal magnetization configuration of the transistor can be obtained. The spin transistor ~~has~~comprises a first electrode structure for injecting spin-polarized carriers, a second electrode structure for receiving the spin-polarized carriers, and a third electrode structure for controlling the ~~amount~~quantity of ~~the~~ spin-polarized carriers ~~conducted~~that are transported from the first electrode structure to the second electrode structure.

The spin ~~transistor is operated based~~transistors operate on the same ~~operating principle as a typical transistor other than the conductive phenomenon depending on the spin. The spin transistor can be classified as a~~principle as that of the conventional transistors with the exception of the involvement of the spin-dependent conduction phenomenon. Thus, the spin transistors can be classified into current-driven ~~type transistor~~transistors such as ~~a~~ bipolar ~~transistor or a~~transistors, and voltage-driven ~~type transistor~~transistors such as ~~an electric~~ field -effect ~~transistor.~~transistors. In terms of the current-driven ~~type~~ transistor, the first electrode structure corresponds to ~~an~~the emitter, the second electrode structure corresponds to ~~a~~the collector, and the third electrode structure corresponds to ~~a~~the base. ~~The spin~~ The spin-filter transistor described ~~in this~~with reference to the present embodiment is ~~classified as the~~a current-driven ~~type.~~transistor. In terms of the voltage~~-driven type~~-driven transistor, the first electrode structure corresponds to the source, the second electrode structure corresponds to the drain, and the third electrode structure corresponds to the gate. The output current in the spin transistor (collector current or drain current) ~~in the spin transistor is changed according to the magnetization state of the ferromagnetic substances included in the spin transistor~~changes depending on the magnetization configuration of the ferromagnet contained in the spin transistor even under the same bias condition.

The details of the spin transistor will be described later. ~~Typical~~ In the following, the general output characteristics of a spin transistors and a nonvolatile memory ~~using the spin transistors will be described. A magnetic field is applied~~employing a spin transistor will be described. It is assumed in the following that the relative magnetization configuration between the free layer and the pin layer can be rendered parallel or antiparallel by applying a magnetic field to the free layer in the spin transistor ~~to make it possible to realize parallel magnetization or anti parallel magnetization of the relative magnetization state of the free layer and the pin layer. The magnetization state can stably exist~~. It is also assumed that the magnetization configuration can exist stably unless a magnetic field ~~above~~exceeding the coercivity of the free layer is applied.

~~FIG~~ Fig. 5 (A) schematically shows an example of ~~an output characteristic of the current driven type spin transistor. Like a typical current driven type~~the output characteristics of a current-driven spin transistor. As in a conventional current-driven transistor, although the collector current I_C can be controlled ~~according to~~by the magnitude of the base current I_B. ~~The magnitude of the collector current depends on the magnetization state of the ferromagnetic substance included in the spin transistor. In FIG. 5(A), when applying~~, it is also dependent on the magnetization configuration of the ferromagnet

contained in the spin transistor. In the example of Fig. 5 (A), even when the bias applied to the spin transistor is the same ~~bias to the spin transistor~~ ($I_B = I_{B1}$), the collector current $I_{C\uparrow\uparrow}$ ~~is large in~~ in the case of parallel magnetization ~~and~~is large, whereas the collector current $I_{C\downarrow\uparrow}$ in the case of antiparallel magnetization is small ~~in anti-parallel magnetization~~.

~~FIG~~Fig. 5 (B) schematically shows an example of ~~an~~the output characteristics of ~~the~~a voltage-driven ~~type~~ spin transistor. ~~Like a~~ As in a conventional field-effect transistor, such as a ~~typical~~ MOS transistor, when ~~a~~the gate- source voltage (V_{GS}) is smaller than the threshold value V_T ($V_{GS} < V_T$), the spin transistor is in ~~the non-conductive~~an off state ~~and a drain current is hardly produced. When applying the V_{GS} above the V_t, the spin transistor is brought to the conductive state. Under the same bias ($V_{GS} = V_{GS1}$), when the ferromagnetic substance included in the spin transistor has~~where hardly any drain current flows. Although the spin transistor conducts when a V_{GS} exceeding V_T is applied, the drain current value differs depending on whether the ferromagnets contained in the spin transistor have parallel magnetization or ~~anti-parallel magnetization, a drain current value is different. In FIG. 3(B), in~~antiparallel magnetization, even under the same bias condition ($V_{GS} = V_{GS1}$). In the case ~~that it has parallel magnetization~~of Fig. 3 (B), the drain current $I_{D\uparrow\uparrow}$ is ~~large, and in the case that it has anti-parallel magnetization,~~larger for parallel magnetization whereas the drain current ~~I_D~~$I_{D\downarrow\uparrow}$ is small for antiparallel magnetization.

~~The~~Thus, the spin transistor, whether it is current-driven or voltage-driven, can electrically detect the magnitude of the relative ~~directions of~~ magnetization configuration of the free layer and the pin layer ~~included in the devices of the current-driven type and the voltage-driven type based on~~contained in the device using the magnitude of the collector current or the drain current. As ~~described~~mentioned above, the ~~ferromagnetic substances can stably hold the direction of magnetization~~relative magnetization configuration in the ferromagnet can exist stably unless a magnetic field ~~above~~exceeding the coercivity of the free layer ~~from outside~~ is externally applied. ~~The~~ Thus, the spin transistor can store~~, in nonvolatile manner,~~ binary information ~~by allowing~~in a nonvolatile manner by rendering the relative magnetization ~~state~~configuration of the free layer and the pin layer ~~included~~contained in the device ~~to be parallel magnetization or anti-parallel magnetization. A one~~-parallel or antiparallel. Therefore, using the spin transistor, a 1-bit nonvolatile memory cell can be ~~const~~fit~~gu~~t~~red only by one~~ with a single spin transistor.

~~Taking the case of using the voltage-driven type spin transistors as an example~~In the following, a nonvolatile memory ~~using the spin transistors~~employing a voltage-driven spin transistor will be described ~~below in detail. A nonvolatile memory using the current-driven type spin transistors as memory cells can be constituted in the same manner~~. The same configuration can be adopted where a current-driven type spin transistor is used in a memory cell.

~~FIG. 6(A) is a diagram showing a structural~~Fig. 6 (A) shows an example of ~~memory cells using spin transistors. FIG. 6(B) is a diagram showing a structural~~the memory cell using the spin transistor. Fig. 6 (B) shows an example of a memory circuit ~~formed based on the memory cells. The relation of FIGS. 6(A) and 6~~configured with the memory cell. The relationship between Fig. 6 (A) and Fig. 6 (B) is the same as that ~~of FIGS~~between Fig. 4 (A) and Fig. 4 (B). In the memory ~~cell~~circuit shown in ~~FIG~~Fig. 6 (A), a number of spin transistors 150 are arra~~y~~nged in a matrix, ~~and source~~with the sources S ~~is~~ grounded ~~to~~

~~connect drain D and gate G to read bit line BL and read word line WL, respectively. A rewrite word line and a rewrite bit line~~and the drains D and the gates G connected to a bitline BL for sensing and a wordline WL for sensing, respectively. A wordline for writing and a bitline for writing are arranged to ~~cross each other on~~intersect one another above the spin transistors 150 in ~~the state of being~~a manner electrically insulated from other wires. ~~As the rewrite word line and the rewrite bit line, the read bit line BL and the read word line WL may be used. FIGS. 6(A) and 6(B) are diagrams showing the structure of this case. In FIGS. 6(A) and 6(B), the memory cell can be constituted by one~~ The wordline for writing and the bitline for writing may be combined with the aforementioned bitline BL for sensing and the wordline WL for sensing, as shown in Fig. 6 (A) and (B). In the case of Fig. 6 (A) and (B), a memory cell can be configured with a single spin transistor ~~and can have~~, and also a very ~~simplified structure for~~simple wiring arrangement can be adopted.

~~In particular,~~Particularly in the case of a voltage-driven ~~type~~ spin transistor ~~having a form~~, which has a similar form to that of a MOS transistor, ~~the source is shared between adjacent memory cells. A~~a layout suitable for microfabrication can be easily ~~constituted~~obtained by, for example, causing adjacent memory cells to use the source in common.

~~The rewrite/read bit line and rewrite/read word line are simply called bit line BL and word line~~The aforementioned writing/sensing bitlines and writing/sensing wordlines will be hereafter referred to simply as a bitline BL and a wordline WL, respectively.

~~Information is rewritten by flowing electric currents to the bit line BL and the word line WL crossing on the~~Information can be written over by causing a current to flow through the bitline BL and the wordline WL that intersect over a selected memory cell ~~to invert~~and then inverting the free layer of the selected memory cell ~~by~~with a ~~synthesized~~composed magnetic field induced by the ~~electric currents flowing to~~current through the respective ~~wires.~~lines. In ~~this case, in~~ order ~~that the~~not to allow non-selected cells connected to the same ~~bit line~~bitline BL or ~~word line~~wordline WL as those of the selected cell ~~is not~~to be inverted by magnetization ~~inverted, current values flowing to the respective wires are set so~~, a current value that is caused to flow in each line is set in advance such that no magnetization inversion ~~does not occur in the~~is caused by a magnetic field ~~from~~emitted by one of the ~~wires~~lines.

~~In reading~~When sensing information, a voltage is applied to the ~~word line~~wordline WL ~~connected to the~~of a selected cell so as to cause the spin transistor to conduct ~~the spin transistor~~, and then a voltage is applied to the ~~bit line~~bitline BL to detect the magnitude of ~~a~~the drain current. Based on the magnitude of the drain current, the relative magnetization ~~state~~configuration of the free layer and the pin layer can be detected. ~~FIG~~

Fig. 6 (B) ~~is a memory circuit connected to output terminal V_O and source voltage V_{DD} branched~~shows the memory circuit shown in Fig. 6 (A), to a bitline end of which an output terminal V_O is connected, with a branch from the output terminal V_O ~~via a load to the bit line end of the memory circuit shown in FIG. 6(A). FIG. 6(C) shows a static characteristic~~connected to a power supply voltage V_{DD} via a load. Fig. 6 (C) shows the static characteristics and operating points of the memory cell shown in ~~FIG~~Fig. 6 (B). ~~Here,~~ Although an active load 160 ~~by a depression~~ consisting of a depletion-type MOS transistor

is used as the load. A in this example, pure resistance may be used, as shown in FIG. 4(B). As shown in FIG. 6(C),Fig. 4 (B). Referring to Fig. 6 (C), when sensing information, a gate voltage V_{GS} is applied to the gate of thea spin transistor 150 at reading information to apply the source voltage V_{DD} via the load to the bit line BL. The operating points by the active load are moved on the load curve in FIG. 6(C) according to the magnetization state ofand a power supply voltage V_{DD} is applied to the bitline BL via a load. This causes the operating point due to the active load to move along the load curve shown in Fig. 6 (C) (between P11 and P12) depending on the magnetization configuration between the pin layer and the free layer (P11 and P12 in the drawing). The output signals V_O in parallel magnetization and anti parallel magnetization are $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$ in the drawing. . As a result, the output signal V_O would be $V_{O\uparrow\uparrow}$ or $V_{O\downarrow\uparrow}$ for the parallel or antiparallel magnetization, respectively. The absolute values andof the ratio of ($V_{O\uparrow\uparrow}/V_{O\downarrow\uparrow}$) of the respective output signals and their ratio ($V_{O\uparrow\uparrow}/V_{O\downarrow\uparrow}$) can be optimized by ausing the transistor characteristics of the active load andor the parameters of the peripheral circuitscircuitry, such as V_{DD}. For instance, the cross point For example, by optimizing the intersection of the static characteristics of the spin transistor and the load curve byof the active load is optimized. When drain current ratio $I_{O\uparrow\uparrow}/I_{O\downarrow\uparrow}$ is small, a large output signal ratio can be obtained. When the values of $I_{O\uparrow\uparrow}$ and $I_{O\downarrow\uparrow}$ are varied by the memory cell and even when the drain current ratio $I_{O\uparrow\uparrow}$ / $I_{O\downarrow\uparrow}$ is small. Further, even if there are variations in the values of $I_{O\uparrow\uparrow}$ and $I_{O\downarrow\uparrow}$ among memory cells, the fluctuation in the output voltage can be almost eliminated as long as the saturation current of the active load is larger than $I_{O\downarrow\uparrow}$ and is$_{\downarrow\uparrow}$ and smaller than $I_{C\uparrow\uparrow}$, the output voltage can be hardly changed. Since$_{\uparrow\uparrow}$. Because no sense amp. isamplifiers are used for readingsensing information, a high speed reading is possible. Thespeed sensing can be performed. Thus, the memory circuit of thisthe present embodiment has the advantages that an output signal havingis advantageous in that output signals of a desired magnitude can be easily obtained and in that a high speed read is possible.sensing can be performed.

In the conventional memory cell usingutilizing the prior art MTJ and MOS transistor, antransistors, output voltages according to produced by the resistance of thea MTJ is readare sensed by a sense amp. Theamplifier. In this case, however, because the output voltage is determined by athe value of the current value flowing tothrough the MTJ and anthe impedance of the MTJ (junction resistance) of, the MTJ. The output voltage ratio cannot be freely adjusted by the peripheral circuitsry.

TheIn the following, the structure of a spin transistor applicable tothat can be used in the nonvolatile memory circuit according to thisof the present embodiment will be described with reference to the drawings. FM is an abbreviation of a, using abbreviations FM for ferromagnetic metal, FS is an abbreviation of anfor electrically conductive ferromagnetic semiconductor, IFS is an abbreviation of anfor insulating ferromagnetic semiconductor, and NM is an abbreviation offor a nonmagnetic substance. An material. In particular, an "NM metal denotes" designates a nonmagnetic metal, and an "NM semiconductor denotes" designates a nonmagnetic semiconductor. The First, a group of spin transistors of the current driven type spin transistors will be described.

FIGFig. 7 isshows an energy band diagram of a hot electron transistor type spin

transistor. A spin transistor 200 ~~has~~comprises an emitter 201 and a base 205 ~~made of~~that are formed by FM or FS. ~~In greater detail~~ Specifically, the spin transistor 200 ~~has the~~comprises emitter 201 ~~made of~~formed by FM (or FS)~~, an~~; emitter barrier 203 ~~made of~~formed by NM~~, the~~; base 205 ~~made of FM (or FS), a~~formed by FM (or FS); collector barrier 207 ~~made of~~formed by NM~~,~~; and ~~a~~ collector 211 ~~made of~~formed by NM. ~~As the~~ NM~~,~~ may be either a nonmagnetic metal or a nonmagnetic semiconductor ~~can be used~~.

In the spin transistor 200 shown in ~~FIG~~Fig. 7, spin-polarized hot carriers are tunnel -injected from the emitter 201 to the base 205 via the emitter barrier ~~203 to the base 205.~~ 203. When the emitter 201 and the base 205 ~~have~~possess parallel magnetization, the injected spin-polarized hot carriers ~~are~~ hardly ~~subject to~~experience spin-dependent scattering ~~in~~within the base 205. ~~When a~~ Thus, by setting the base width ~~is set so~~such that the ~~spin-polarized hot~~ carriers can ~~be ballistically transmitted~~pass through the base ~~205, they cross over~~205 ballistically, the carriers can be transported beyond the collector barrier 207 to the collector 211. ~~The same~~ This is a transistor operation ~~as~~similar to that of a ~~typical~~conventional hot electron transistor ~~is performed~~.

~~When~~On the other hand, when the emitter 201 and the base 205 ~~have anti-parallel~~possess antiparallel magnetization, the spin-polarized hot carriers injected from the emitter 201 ~~into~~to the base 205 lose energy ~~by~~due to the spin-dependent scattering ~~in~~within the base 205 ~~to be a base current without crossing over~~and are therefore unable to overcome the collector barrier ~~207. When~~207, resulting in a base current. Namely, when the emitter 201 and the base 205 ~~have anti-parallel magnetization, the current transmission factor is lower than the case that both have parallel magnetization. When applying the same bias~~possess antiparallel magnetization, the current transfer ratio drops as compared with the case of parallel magnetization. Therefore, even if the same bias is applied to the spin transistor 200, the current transfer ratio or current gain varies depending on the difference in the relative magnetization ~~state of~~configuration between the emitter 201 and the base ~~205 makes the current transmission factor or the current amplification factor different.~~ 205. The spin transistor 200 can be operated at room temperature by ~~suitably~~appropriately selecting the collector barrier height ~~of the collector barrier. The spin transistor 200 must have a large base width~~, for example.

In the spin transistor 200, if the ratio of the current transfer ratio in the case where the emitter-base junction has parallel magnetization and that in the case where the junction has antiparallel magnetization is to be increased, the base width must be sufficiently large so that the spin-dependent scattering can effectively function ~~to increase the ratio of the current transmission factors in the case that the emitter and the base have parallel magnetization and the case that they have anti-parallel magnetization. When the base width is increased and the emitter and the base have parallel magnetization, the current transmission factor is smaller and is below 0.5 so that a trade-off in which the~~. However, when the base width is increased, the current transfer ratio becomes smaller even when the emitter-base junction has parallel magnetization, dropping below 0.5, for example. Thus, there is a tradeoff between an increase in the base width and a decrease in amplification function ~~is lost exists~~.

~~FIG~~Fig. 8 ~~is~~shows an energy band diagram of a hot -electron transistor type spin transistor ~~using thermal release as a spin injection~~in which thermionic emission is utilized

as a mechanism ~~to a~~for injecting spin polarized carriers to the base. As shown in ~~FIG~~Fig. 8, a spin transistor 220 ~~has~~comprises an emitter 221 ~~made of~~formed by FM (or FS)~~,~~; a base 225 ~~made of~~formed by FM (or FS)~~,~~; and an emitter barrier 223 ~~made of NM provided between both. It further has a collector barrier 227 of NM, and a collector 231 of NM~~disposed between the emitter and the base and formed by NM. Furthermore, on the opposite side ~~of~~to the junction ~~of~~between the base 225 and the emitter barrier ~~223. A nonmagnetic semiconductor can be used for the~~223, there is provided a collector barrier 227 formed by NM and a collector 231 formed by NM. The emitter barrier 223 and ~~the~~ collector barrier ~~227. A~~227 may be formed by a nonmagnetic semiconductor. The collector 231 may be formed by a nonmagnetic metal ~~can be used for the collector 231.~~.

~~An~~Between the emitter 221 and the emitter barrier 223, an ohmic contact or a tunnel contact is formed ~~between~~. Between the ~~emitter 221~~base 225 and the emitter barrier ~~223. A junction is formed between the base 225 and the emitter barrier 223 or~~223, and between the base 225 and the collector barrier ~~227 so as to have~~227, a junction exhibiting a band discontinuity as shown in ~~FIG. 9. The~~Fig. 9 is formed. This band discontinuity can be realized by a Schottky junction between ~~the~~ NM semiconductor and FM ~~and~~, or by a heterojunction between ~~the~~ NM semiconductor and FS. Alternatively, a Schottky junction ~~is~~may be formed ~~of~~between FS and FM, ~~a~~and the resultant Schottky barrier ~~produced in this case is an~~may be used as the emitter barrier, with FS ~~is an emitter,~~ and FM ~~is a~~functioning as emitter and base, respectively.

The spin-polarized carriers diffused from the emitter 221 to the emitter barrier 223 ~~by applying~~through the application of a bias to the base 225 with respect to the emitter 221 are injected to the base 225 as hot carriers ~~into the base 225 by thermal release.~~by thermionic emission. When the emitter 221 and the base 225 ~~have~~possess parallel magnetization, the spin-polarized hot carriers injected into the base 225 can reach the collector without being ~~subject to spin dependent scattering. When~~subjected to spin-dependent scattering. However, when the emitter 221 and the base 225 ~~have anti-parallel~~possess antiparallel magnetization, the spin-polarized hot carriers ~~become~~are rendered into a base current by spin-dependent scattering~~. The spin~~. In this transistor 220 ~~uses~~too, because it utilizes spin-dependent scattering in the base~~. Like the~~, there is a tradeoff, as in the above-described spin transistor 200, ~~a trade off relation exists~~ between the ratio of the current ~~transmission factors~~transfer ratio in the case of parallel magnetization and ~~anti-parallel~~that in the case of antiparallel magnetization, and the current ~~transmission factor in~~transfer ratio in the case of parallel magnetization. ~~As~~ The transistor 220, however, is advantageous as compared with the spin transistor ~~200 using~~200, which utilizes tunnel injection, ~~there are characteristics~~in that a larger current driving force can be ~~large~~obtained and in that a room-temperature operation can be easily realized.

~~FIG~~Fig. 9 ~~is~~shows an energy band diagram of a hot-electron transistor type spin transistor ~~using~~utilizing the spin-filter effect. Although the transistor ~~is~~has already been described in detail, its characteristics will be briefly described. A spin transistor 240 shown in ~~FIG~~Fig. 9 ~~has~~comprises an emitter barrier 243 and a collector barrier 247 ~~made of~~that are formed by IFS. ~~From~~ Via an emitter ~~241 made of~~241, which is formed by an NM semiconductor (or an NM metal), ~~only~~the carriers ~~having one of spins by the spin filter~~

~~effect of the emitter barrier 243~~with one spin can be selectively injected into ~~a~~the base ~~245 made of~~245, which is formed by an NM semiconductor (or an NM metal)~~. The~~, through the spin-filter effect provided by the emitter barrier 243. When the base width is set ~~below~~to be not greater than the mean free path of the spin-polarized hot carriers~~.~~, ~~T~~the spin-polarized hot carriers injected into the base 245 are transported to the base 245 ballistically ~~conducted through the base 245. At~~. In this ~~time~~case, the spin transistor 240 is biased ~~so~~such that the spin-polarized hot carriers are injected into the energy -split width ~~of the~~between an up -spin band ~~of the collector barrier 247 (the~~(a spin band edge ~~indicated~~designated by the upward arrow in ~~FIG~~Fig. 9) and ~~the~~a down -spin band (~~the~~a spin band edge ~~indicated~~designated by the downward arrow in ~~FIG~~Fig. 9). When the emitter barrier 243 and the collector barrier 247 have parallel magnetization, the spin-polarized hot carriers injected into the base 245 ~~cross~~can overcome the barrier ~~by~~of the spin band ~~having a low~~of lower energy in the collector barrier 247 ~~by~~through the spin -filter effect of the collector barrier ~~247~~247, and ~~can be propagated~~therefore propagate to a collector ~~251 of~~251, which is formed by an NM semiconductor (or an NM metal). ~~When~~ On the other hand, when the emitter barrier 243 and the collector barrier 247 have ~~anti-parallel~~antiparallel magnetization, most of the spin-polarized hot carriers ~~become a base current without crossing over~~cannot overcome the collector barrier 247 ~~by the spin filter effect of the collector barrier 247.~~because of the spin-filter effect of the collector barrier 247, resulting in a base current.

~~In~~Thus, in the spin transistor 240, the current ~~transmission factor~~transfer ratio (or the current ~~amplification factor) is different according to~~gain) differs depending on the relative ~~directions of~~ magnetization configuration of the emitter barrier 243 and the collector barrier 247. ~~The~~ Because the spin -filter effect ~~has~~provides a very ~~large~~high spin -selectivity~~. The ratio of the current transmission factors in~~, the ratio of current transfer ratio in the case of parallel magnetization and ~~anti-parallel~~that in the case of antiparallel magnetization can be increased ~~in the transistor~~.

~~The spin transistor 240 can sufficiently decrease the base width.~~ ~~Unlike~~Furthermore, in the spin transistor ~~using spin~~ 240, the base width can be made sufficiently small. Therefore, in contrast to the spin transistor that utilizes spin-dependent scattering, as in the cases shown in ~~FIGS. 7 and 8, there is the advantage that a trade-off related to the base width~~Figs. 7 and 8, the spin transistor 240 is advantageous in that there is no tradeoff between the current ~~amplification factor~~gain relating to the base width and the spin selectivity ~~does not exist~~.

~~FIG~~Fig. 10 ~~is~~shows an energy band diagram of a tunnel base transistor type spin transistor. As shown in ~~FIG~~Fig. 10, ~~in~~ a tunnel base transistor type spin transistor ~~260, a p-type (or n-type) FS is used for~~260 comprises an emitter 261 and a collector 265 ~~and an n-type (or p-type) NM semiconductor is used for a tunnel base 263. It is preferable to use~~that are formed by a p-type (or an n-type) FS, and a tunnel base 263, which is formed by an n-type (or a p-type) NM semiconductor. In the emitter-base junction and in the base-collector junction, a heterojunction of type II is preferably used so that the base 263 ~~is~~becomes a barrier to the holes (or electrons) ~~between the emitter and the base and between the base and the collector~~. The base width is ~~smaller so as to produce a tunnel~~reduced sufficiently that a tunneling current from the emitter to the collector is produced.

In the structure shown in ~~FIG~~Fig. 10, when the emitter 261 and the collector 265 have parallel magnetization, the carriers ~~having a number of spins of~~with the majority spin in the emitter can be easily ~~tunneled~~transported to the collector 265 ~~and~~through tunneling, namely, the tunnel conductance is large. ~~When~~ However, when the emitter 261 and the collector 265 have ~~anti-parallel~~antiparallel magnetization, the tunnel conductance is ~~small~~reduced by the tunneling magnetoresistance (TMR) effect ~~(TMR effect). The~~. Thus, the magnitude of the collector current can be controlled ~~according to~~by the relative magnetization ~~state of~~configuration between the emitter 261 and the collector 265.

~~When~~If the TMR ratio in the spin transistor 260 can be ~~large~~increased, the change in ~~the~~ collector current ~~depending~~that depends on the magnetization ~~state of the~~configuration between emitter and ~~the~~ collector can be increased. ~~To effectively exhibit~~ In order to allow the TMR effect ~~by~~to be effectively exhibited in the spin transistor 260, ~~preferably, a depression layer is not expanded to~~it is preferable to prevent the depletion layer from expanding towards the collector ~~side~~ when ~~applying~~ a reverse bias ~~to~~is applied across the base--collector junction. ~~When the depression~~ It is noted, however, that if the depletion layer is expanded ~~to~~towards the base ~~side, the possibility that,~~ a problem ~~arises in the saturation characteristic of~~could possibly arise in the collector current ~~exists~~saturation characteristics.

When the base layer ~~is doped with high density so as not to expand the depression layer to the base layer~~ in the spin transistor 260 ~~and the depression layer of~~is heavily doped so as to prevent the spreading of the depletion layer and to cause the depletion layer in the base--collector junction ~~is expanded~~ to spread towards the collector ~~side~~, the TMR effect in the base cannot be expected ~~and~~. However, the carriers injected into the collector ~~produce resistance by~~are subjected to spin--dependent scattering in the collector. ~~Using the spin~~ resistance, resulting in increased resistance. By utilizing this spin-dependent scattering ~~can change~~, the magnitude of the collector current ~~according to~~can be varied by the magnetization ~~state of the emitter and the collector. The change in resistance by the spin~~ configuration in the emitter-collector junction. It is possible, however, that the effect is not so large as that obtained with the TMR effect because the resistance change through spin-dependent scattering is small. ~~As compared with using the TMR effect, the effect may be not high.~~

~~The~~Hereafter, a group of voltage--driven ~~type~~ spin transistors will be described with reference to the drawings.

~~FIG~~Fig. 11 ~~is a diagram showing the~~shows a cross ~~sectional structure~~-section of a MOS transistor type spin transistor. As shown in ~~FIG~~Fig. 11, ~~a~~the MOS transistor type spin transistor 300 ~~has a structure in~~comprises an NM semiconductor 301 on which a source 303 ~~made of~~formed by FM, a drain 305 ~~made of~~formed by FM, and a gate electrode 311 are formed, the gate electrode via a gate ~~insulator film 307 are formed on an NM semiconductor 301.~~ insulating film 307. A Schottky junction of ~~the~~ FM and an NM semiconductor is used for the source 303 and the drain 305. ~~Other structure is~~ The other structures are the same as ~~that of a typical~~those of a conventional MOS transistor.

Spin--polarized carriers injected from the source 303 into a channel formed directly below the gate insulat~~or~~ing film 307 ~~in~~of the NM semiconductor 301 pass

through the channel to the drain 305 (~~hereinafter, for simplification~~hereafter, the influence of the Rashba effect ~~by~~due to the gate electric field of the spins injected into the channel ~~is neglected).~~will be ignored for simplicity). When the source 303 and the drain 305 have parallel magnetization, the spin-polarized carriers injected into the drain 305 are not subject to spin-dependent scattering. When they have ~~anti-parallel~~antiparallel magnetization, however, resistance by spin-dependent scattering is produced in the drain electrode 305.

~~In~~Thus, in the transistor 300, the mutual conductance ~~is different according to~~differs depending on the relative ~~directions of~~ magnetization ~~of~~configuration between the source and ~~the~~ drain.

~~FS can be also used for the~~The source 303 and the drain 305 ~~to form~~may be formed by FS, and a pn junction is formed between ~~it~~each and the semiconductor ~~301 to form a source and a drain.~~301.

~~FIG~~Fig. 12 ~~is a diagram showing the~~shows a cross-~~sectional structure~~ section of a modulation -doped transistor type spin transistor. ~~A~~ The spin transistor 320 ~~has~~comprises a source 323 ~~made~~ of FM (or FS) ~~to a~~in contact with the two-dimensional carriers gas produced at the ~~interface of~~boundary between a first NM semiconductor 321 and a second NM semiconductor ~~327,~~327; a drain 325 ~~made of~~formed by FM (or FS)~~,~~; and a gate electrode 331. ~~It is the same as a typical modulation dope transistor except~~ The spin transistor 320 is identical to a conventional modulation-doped transistor with the exception that the source 323 and ~~the~~ drain 325 are ~~made of ferromagnetic substances~~formed by a ferromagnet.

Spin-polarized carriers are injected from the source 323 ~~into~~to a channel 333 formed by the two-dimensional carrier gas. The spin-polarized carriers ~~which have reached~~that reach the drain 325 have different mutual conductance ~~according to~~depending on the relative ~~directions of~~ magnetization configuration of the source 323 and the drain 325 due to spin-dependent scattering in the drain 325.

~~FIG~~Fig. 13 ~~is~~shows a cross-~~sectional view~~ section of a MOS transistor type spin transistor ~~using FS for a~~in which the channel region. ~~A~~ is formed by FS. The spin transistor 340 shown in ~~FIG~~Fig. 13 ~~has a structure in~~comprises FS 341 on which a source 343 ~~made of~~formed by FM, a drain 345 ~~made of~~ formed by NM (or FM or FS), and a gate electrode 351 via a gate insulat~~or~~ing film 347 are formed ~~on an FS 341.~~. A Schottky junction of ~~the~~ FM and FS is used ~~for the source 343. Other structure is the same as that of a typical~~in the source 343; except for that, the structure is identical to that of a conventional MOS transistor.

Spin-polarized carriers are ~~tunnel~~ injected from the source 343 ~~via~~into the channel 341 by tunneling through the Schottky barrier ~~into the channel 341. The~~. Based on the TMR effect and the spin-dependent scattering in the channel of FS341 during tunneling injection, a mutual conductance ~~depending~~that depends on the relative ~~directions of~~ magnetization configuration of the source 343 and ~~the~~ FS 341 is realized ~~by the TMR effect at the tunnel injection and spin-dependent scattering in the channel of the FS 341.~~.

~~A~~Fig. 14 shows a cross section of a spin transistor 360 ~~showing its cross-sectional structure in FIG. 14 is a spin transistor having~~comprising a tunnel junction structure ~~interposing~~in which an insulating NM tunnel barrier 365 is disposed between a source 361

made offormed by FM (or FS) and a drain 363 made offormed by FM (or FS) and arranging a. It is a spin transistor with the gate electrode 371 so as to applydisposed such that an electric field can be applied to the tunnel barrier 365.

The film thickness of the tunnel barrier 365 is preferably set to a thickness sosuch that no Fowler--Nordheim (FN) tunneling occurs when applying only a bias between the source and the drain. The bias is applied. A triangular potential at the band edge of the tunnel barrier band edge produced by applying a bias betweenacross the source and the drain junction is changedvaried by athe gate voltage in order to induce the FN tunneling to and obtain a drain current.

Spin-polarized carriers injected from the source 361 are subject to spin-dependent scattering in the drain 363 according todepending on the relative magnetization stateconfiguration of the source 361 and the drain 363. The Thus, the mutual conductance of the transistor can be controlled by the relative directions of magnetization ofconfiguration between the source and the drain.

AFig. 15 shows a cross section of a spin transistor 380 showing its cross-sectional structure in FIG. 15 replaces the tunnel barrier of380, which is similar to the spin transistor 360 shown in FIGFig. 14 with the exception that the tunnel barrier comprises a tunnel barrier 385 made offormed by IFS. A While a source 381 must be of FM or FS. A, a drain 383 needmay not be a ferromagnetic substance. The barrier height offerromagnet. In the IFS tunnel barrier layer 385 is different according to the385, the barrier height differs depending on the spin direction of the spin of carriers. When the source 381 and the tunnel barrier 385 have parallel magnetization, a bias iscarriers. A bias is therefore applied between the source and the drain and betweenacross the source and the gate sojunction such that the transistor is brought to the conductive state.conducts when the source 381 and the tunnel barrier 385 have parallel magnetization. Under the same bias condition, when the source 381 and the tunnel barrier 385 have anti parallelantiparallel magnetization, the tunnel barrier height of the tunnel barrieras seen from a number of spins ofthe majority spin in the source 381 is increased. The tunnelincreases. As a result, the tunneling probability of the spin-polarized carriers is decreased to reduce thedecreases, leading to a decrease in drain current. The spin selectivity by the spin filter effect is very large. When using a ferromagnetic substance having a large spin polarizability as the source 381, the mutual conductance according to Because the spin selectivity provided by this spin-filter effect is extremely large, the change in mutual conductance depending on the relative directions of magnetization configuration of the source and the drain can be largely changed.increased by using a ferromagnet with a large spin polarization in the source 381.

TheAny of the above-described various spin transistors canmay be used as the memory cells for the memory circuit shown in FIGFig. 4 or FIGFig. 6.

It is also possible to form a structureconfiguration in which the sources of the two voltage-driven type spin transistors shown in FIGSFigs. 11, 1414, and 15 are shared as one source. FIG. 16(A) is a diagram showing a structural example of memory cells having a shared source structure. FIG. 16(B) is a diagram showing a cross sectional structural examplehave a common source. Fig. 16 (A) shows an example of a memory cell of a common-source configuration. Fig. 16 (B) shows a cross section of the memory cells having a shared of a common-source structure. configuration.

The memory cell structure shown in ~~FIGS~~Figs. 16 (A) and ~~16~~(B) ~~has~~comprises a first spin transistor Tr1 and a second spin transistor Tr2 that are disposed adjacent ~~each other, word line WL sharably~~to one another; a wordline WL connecting a gate electrode G1 of the first spin transistor Tr1 and a gate electrode G2 of the second spin transistor Tr~~2~~2; a first ~~bit line~~bitline BL1 connected to a first drain D1 of the first spin transistor Tr~~1~~1; a second ~~bit line~~bitline BL2 connected to a second drain D2 of the second spin transistor~~,~~; a ferromagnetic source S ~~shared between~~common to the first and second spin transistors Tr1 and Tr~~2, and a wire grounding it. Using the above structure shares the source provides a~~2; and a line connecting the common source to ground. In this configuration, the common source makes the cell structure suitable for higher -density integration.

~~To minimize a leak current at non-conduction, in~~In particular, the voltage-driven ~~type~~ spin transistors shown in ~~FIGS. 11, 14 and 15, it is preferable to use~~Figs. 11, 14, and 15 preferably comprise a highly insulating substrate, such as an SOI substrate ~~having a high insulation,~~ as shown in ~~FIG. 16(B).~~ Fig. 16 (B), so as to reduce leakage current when the transistor is off.

As described above, the spin -filter transistor ~~according to the embodiments of the present invention~~ and various spin transistors ~~shown in this embodiment have a characteristic capable of controlling an output characteristic according to the relative directions of magnetization of the pin layer and the~~according to the various embodiments of the present embodiment are characterized in that the output characteristics can be controlled by the relative magnetization configuration of the pin layer and free layer ~~included in~~within the device. The relative magnetization ~~state has a nonvolatile characteristic capable of holding the state without supplying an electric power. The relative magnetization states can be stored as~~configuration is nonvolatile, namely, the device does not require the feeding of power for retaining the magnetization configuration. Thus, the device can store binary information in ~~nonvolatile manner. Using the above output characteristic can electrically detect~~terms of the relative magnetization ~~state. A one~~-configuration in a nonvolatile fashion. Further, using the aforementioned output characteristics, the relative magnetization configuration can be electrically detected. Thus, a 1-bit nonvolatile memory cell can be const~~f~~itgut~~r~~ed ~~only by one~~ with a single spin transistor. Using ~~the~~a nonvolatile memory circuit ~~using the~~comprising a spin transistor according to ~~this embodiment can freely design the magnitude of output signals and~~the embodiments of the invention, the ratio of output signals ~~to~~as well as their magnitudes with respect to the stored information can be freely designed.

~~Using~~Thus, using the spin transistor according to thi~~s~~e embodiments of the ~~present~~ invention and a memory circuit ~~using the same can increase~~comprising the spin transistor, the operating speed and the level of integration of ~~the~~a nonvolatile memory circuit can be increased.

~~The~~While the present invention ~~is~~has been described ~~above along the~~with reference to various embodiments~~. The~~ thereof, the present invention is not limited ~~to these. It is apparent~~by any of these embodiments. It should be obvious to those skilled in the art that various modifications, improvements ~~and~~or combinations can be made.

INDUSTRIAL APPLICABILITY

~~As described above,~~In accordance with the spin -filter transistor of the present invention ~~can largely change an output characteristic according to~~, the output characteristics can be greatly changed by the relative ~~directions of~~ magnetization ~~of~~configuration of the ferromagnetic barrier layers.

~~The~~A nonvolatile memory circuit ~~using, as~~comprising a memory ~~cells, the~~cell employing this spin -filter transistor ~~and another~~or a spin transistor ~~having a characteristic equal to that of this~~with equivalent characteristics can store binary information ~~according to~~in terms of the relative ~~directions of~~ magnetization ~~of ferromagnetic substances included~~configuration of ferromagnets contained in the transistor ~~and can electrically detect the~~. The relative ~~directions of~~ magnetization. ~~Using~~ configuration can also be detected electrically. Furthermore, using the nonvolatile memory circuit of the present invention ~~can freely design~~, the output signals with respect to the stored information. ~~A high~~ can be freely designed. Using such a spin transistor, a high-speed and high integration-density nonvolatile memory circuit ~~with high density integration constituting a one~~ can be realized that comprises a 1-bit nonvolatile memory cell ~~only by one~~made up of a single transistor ~~can be realized.~~.

CLAIMS

1. A transistor comprising :

a spin injector for injecting spin-polarized hot carriers by a spin -filter effect~~,~~; and

a spin analyzer for selecting the thus injected spin-polarized hot carriers by the spin -filter effect.

2. The transistor according to claim 1, wherein said spin injector ~~has~~ comprises:

a first ferromagnetic barrier layer ~~capable of tunneling carriers by applying a voltage at both ends,~~ through which the carriers can be transported by tunneling upon application of a voltage across said first ferromagnetic barrier layer;

a first nonmagnetic electrode layer joined to one end surface of said first ferromagnetic barrier layer~~,~~; and

a second nonmagnetic electrode layer joined to the other end surface of said first ferromagnetic barrier layer.

3. The transistor according to claim 1 or 2, wherein said spin analyzer ~~has~~ comprises:

a second ferromagnetic barrier layer~~,~~;

said second nonmagnetic electrode layer joined to one end surface of ~~the~~said second ferromagnetic barrier layer~~,~~; and

a third nonmagnetic electrode layer joined to the other end surface of said second ferromagnetic barrier layer, ~~and shares~~wherein said second nonmagnetic electrode layer ~~with~~is common to said spin injector and said spin analyzer.

4. The transistor according to claim 2 or 3, wherein said first and second ferromagnetic barrier layers ~~include~~comprise a ferromagnetic semiconductor or a ferromagnetic insulator.

5. The transistor according to any one of claims 1 to 4, wherein the thickness of said second nonmagnetic electrode layer is ~~below~~smaller than the mean free path of the spin-polarized hot carriers ~~of~~in said second nonmagnetic electrode layer.

6. ~~The~~A transistor according to any one of claims 1 to 5, wherein ~~according to~~ the spin -filter effect of said spin injector~~, in the tunnel effect of the carriers~~ takes advantage of the fact that, in a carrier tunneling effect in said first ferromagnetic barrier layer which is produced ~~by applying~~through the application of a voltage to said first nonmagnetic electrode layer and to said second nonmagnetic electrode layer, ~~large is the tunnel probability~~those of the carriers ~~having the~~that exist in said first nonmagnetic electrode layer and that have a spin direction ~~of the spin~~ parallel to ~~the~~a spin band at the band edge of said first ferromagnetic barrier layer ~~of the carriers existing in said first nonmagnetic electrode layer, and small is the tunnel probability of the carriers having the direction of the spin anti-parallel thereto~~have a large tunneling probability, while those carriers with an antiparallel spin direction have a small tunneling probability.

7. The transistor according to any one of claims 1 to 6, wherein ~~according to~~ the spin -filter

effect of said spin analyzer takes advantage of the fact that, when the spin direction of the spin ~~of spin~~-polarized hot carriers injected from said spin injector is parallel to ~~the direction of the spin~~that of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers are ~~conducted~~transported through the spin band at the band edge of said second ferromagnetic barrier layer ~~to~~and reach said third nonmagnetic electrode layer, ~~and~~whereas when the spin direction of ~~the spin of~~ said spin-polarized hot carriers is ~~anti-parallel to the direction of the spin~~antiparallel to that of the spin band at the band edge of said second ferromagnetic barrier layer, said spin-polarized hot carriers ~~cannot~~are unable to reach said third nonmagnetic electrode layer.

8. The transistor according to any one of claims 1 to 7, wherein a first voltage is applied ~~by a first power source~~ between said first nonmagnetic electrode layer and said second nonmagnetic electrode layer~~,~~ from a first power supply, and a second voltage is applied ~~by a second power source~~ between said second nonmagnetic electrode layer and said third nonmagnetic electrode layer or between said first nonmagnetic electrode layer and said third nonmagnetic electrode layer, ~~and according to the relative directions of magnetization of said first ferromagnetic barrier layer and said second ferromagnetic barrier layer, spin~~ from a second power supply, and wherein said spin-polarized hot carriers injected from said first nonmagnetic electrode layer ~~into~~to said second nonmagnetic electrode layer are switched to ~~either an electric~~a current ~~flowing via~~through said second ferromagnetic barrier layer and said second power ~~source~~supply or ~~an electric~~a current ~~flowing via~~through said second nonmagnetic electrode layer and said first power ~~source.~~ supply depending on the relative magnetization configuration of said first ferromagnetic barrier layer and said second ferromagnetic barrier layer.

9. The transistor according to claim 8, wherein said first voltage is applied ~~so~~such that the energy of the injected spin-polarized hot carriers ~~is~~becomes larger than the ~~energy of the~~ spin band edge ~~of~~energy at the band edge of the said second ferromagnetic barrier layer and ~~is~~ smaller than the energy ~~in~~of the spin band edge to which ~~a~~the spin -split width is added ~~to the energy of the spin band edge~~.

10. The transistor according to claim 9, wherein ~~a magnetic field is applied to invert any one of the directions of~~the relative magnetization ~~of~~configuration in said first ferromagnetic barrier layer ~~and~~or said second ferromagnetic barrier layer can be reversed with the application of a magnetic field.

11. A memory circuit ~~wherein~~comprising a memory cell formed by the transistor according to any one of claims 1 to ~~10 is a memory cell.~~10.

12. The memory circuit according to claim 11, wherein ~~the~~said second nonmagnetic electrode layer of said transistor is connected to a ~~word line, the~~wordline, said third nonmagnetic electrode layer of said transistor is connected to a ~~bit line~~bitline, said ~~bit line~~bitline is connected ~~via a load~~ to a power ~~source~~supply via a load, and ~~the~~said first nonmagnetic electrode layer of said transistor is ~~grounded~~connected to ground.

13. A ~~storage device~~memory element comprising:

a transistor ~~(hereinafter, called a "spin transistor") including ferromagnetic substances~~containing a ferromagnet and having ~~an~~ output ~~characteristic depending~~characteristics that depend on the spin direction of ~~the spin of~~ carriers (to be hereafter referred to as a "spin transistor");

an information ~~rewriting means rewriting information in~~writing means for writing information within said spin transistor by changing the magnetization ~~state~~configuration of said ~~ferromagnetic substances~~ferromagnet; and

an information ~~reading~~sensing means ~~reading~~for sensing from said output characteristics information stored in said spin transistor ~~as the~~in terms of a magnetization ~~state from said output characteristic~~configuration.

14. The ~~storage device~~memory element according to claim 13, wherein said spin transistor ~~has at least one ferromagnetic substance (hereinafter, called a "free layer") capable of independently controlling the direction of magnetization and at least one ferromagnetic substance (hereinafter, called a "pin layer") not changing the direction of magnetization, and holds any one of two stored states of~~comprises at least one ferromagnet in which the relative magnetization configuration can be independently controlled (to be hereafter referred to as a "free layer"), and a ferromagnet in which the relative magnetization configuration is not changed (to be hereafter referred to as a "pin layer"), wherein

one of two memory states, namely, a first state in which said free layer and said pin layer have the same ~~direction of~~relative magnetization configuration, and a second state ~~having~~in which they have different ~~directions of~~ magnetization configurations, is retained.

15. A ~~storage device~~memory element according to claim 14, wherein ~~one~~a single spin transistor ~~according to claim 14 is used to store~~stores information ~~according to~~in terms of the relative ~~directions of~~ magnetization ~~of~~configuration of said free layer relative to said pin layer, and ~~said free layer for detecting the~~wherein information stored in said transistor ~~based on an~~is detected using the output characteristics of said spin transistor ~~depending~~, which depend on the relative ~~directions of~~ magnetization configuration of said pin layer and said free layer.

16. The ~~storage device~~memory element according to claim 14 or 15, wherein said spin transistor ~~has~~comprises: a first electrode structure for injecting spin-polarized carriers~~,~~;

a second electrode structure for receiving said spin-polarized carriers~~,~~; and

a third electrode structure for controlling the ~~quantity~~amount of the spin-polarized carriers ~~conducted~~transported from said first electrode structure to said second electrode structure, ~~and~~ wherein

said pin layer and said free layer are included in any ~~one~~ of said first to third electrode structures.

17. A ~~storage device~~memory element comprising:

~~one~~a single spin transistor ~~according to~~described in claim 16;

a first ~~wire grounding~~line connecting said first electrode structure to ground;

a second ~~wire~~line connected to said second electrode structure; and

a third ~~wire~~line connected to said third electrode structure.

18. A ~~storage device~~memory element comprising:

~~one~~a single spin transistor according to claim 16;

a first ~~wire grounding~~line connecting said first electrode structure to ground;

~~a second wire connected to said second electrode structure;~~

~~a third wire connected to said third electrode structure;~~

a second line connected to said second electrode structure;

a third line connected to said third electrode structure;

an output terminal formed at one end of said second ~~wire~~line; and

a fourth ~~wire~~line branch~~ed~~ing from said second ~~wire to be~~line and connected ~~via a load~~ to a power ~~source~~supply via a load.

19. The ~~storage device~~memory element according to claim 17 or 18, further comprising a first ~~another wire~~separate line and a second separate line that intersect one another ~~wire crossing on~~above said spin transistor ~~to be~~in an electrically insulated ~~from each other~~manner.

20. The ~~storage device~~memory element according to claim 19, wherein ~~in place of~~ said first ~~another wire and said second another wire or any one of said first another wire and said second another wire, said second wire and said third wire are used or any one of said second wire~~separate line and/or said second separate line are replaced with said second line and/or said third ~~wire is used~~line.

21. The ~~storage device~~memory element according to claim 19 or 20, wherein information is written by reversing the magnetization of said free layer by a magnetic field induced by ~~flowing electric currents to~~causing a current to flow through said first ~~another wire~~separate line and said second ~~another wire~~separate line, or through said second ~~wire~~line and said third ~~wire inverts the magnetization of said free layer to change~~line, thereby changing the relative magnetization ~~state of~~configuration between said pin layer and said free layer ~~for rewriting information~~.

22. The ~~storage device~~memory element according to claim 17 or 18, wherein information is ~~read based on an~~sensed using the output characteristics of said spin transistor when ~~applying~~ a first bias is applied to said third ~~wire~~line and a second bias is applied between said first ~~wire~~line and said second ~~wire~~line.

23. The ~~storage device~~memory element according to any one of claims 18 to 22, wherein ~~when applying a first bias to said third wire,~~ information is ~~read by~~sensed using an output voltage that is obtained ~~based~~ on the basis of a voltage drop ~~of~~across said load ~~produced~~due

to a current through said load and said spin transistor between said power ~~source~~supply and said first ~~wire and said load by an electric current via said spin transistor~~line when a first bias is applied to said third line.

24. A memory circuit comprising:

~~one~~a single spin transistor according to claim 16 arra~~y~~nged in a matrix;

a first ~~wire grounding~~line connecting each ~~of said~~ first electrode ~~structures~~structure to ground;

a plurality of ~~word lines sharably~~wordlines commonly connecting said third electrode structures of said spin transistors arra~~y~~nged in the column direction; and

a plurality of ~~bit lines sharably~~bitlines commonly connecting said second electrode structures of said spin transistors arra~~y~~nged in the row direction.

25. A memory circuit comprising:

~~a~~the spin transistor according to claim 16 arra~~y~~nged in a matrix;

a first ~~wire grounding~~line connecting each ~~of said~~ first electrode ~~structures~~structure to ground;

a plurality of ~~word lines sharably~~wordlines commonly connecting said third electrode structures of said spin transistors arra~~y~~nged in the column direction;

a plurality of ~~bit lines sharably~~bitlines commonly connecting said second electrode structures of said spin transistors arra~~y~~nged in the row direction;

an output terminal formed ~~at~~on one end of said ~~bit line~~bitlines; and

a second ~~wire~~line branch~~ed~~ing from said ~~bit line to be~~bitline and connected ~~via a load~~ to a power ~~source~~supply via a load.

26. The memory circuit according to claim 24 or 25, further comprising a first ~~another wire~~separate line and a second separate line that intersect one another ~~wire crossing on~~above said transistor ~~to be~~in an electrically insulated ~~from each other~~manner.

27. The memory circuit according to claim 26, wherein ~~in place of~~ said first ~~another wire~~separate line and/or said second ~~another wire or any one of said first another wire and said second another wire, said word line and said bit line are used or any one of said word line~~separate line are replaced with said wordline and/or said ~~bit line is used~~bitline.

28. The memory circuit according to claim 26 or 27, wherein ~~a magnetic field induced by flowing electric currents to said first another wire and said second another wire or said word line and said bit line inverts~~information is written by reversing the magnetization of said free layer ~~to change~~by a magnetic field induced by causing a current to flow through said wordline and said bitline, thereby changing the relative magnetization ~~state of said free layer and~~configuration between said pin layer ~~for rewriting information~~and said free layer.

29. The memory ~~circuit~~element according to claim 24 or 25, wherein information is ~~read based on an~~sensed using the output characteristics of said spin transistor when ~~applying~~ a first bias is applied to said ~~word line~~wordline and a second bias is applied between said first

~~wire~~line and said ~~bit line.~~ bitline.

30. The memory ~~circuit~~element according to any one of claims 25 to 27, wherein ~~when applying a first bias to said word line,~~ information is ~~read by~~sensed using an output voltage that is obtained ~~based~~ on the basis of a voltage drop ~~of said load produced~~across said load due to a current through said load and said spin transistor between said power ~~source~~supply and said first ~~wire and said load by an electric current via said spin transistor~~line when a first bias is applied to said third line.

31. A ~~storage device~~memory element comprising:

a first and a second spin transistors according to claim 16;

a first ~~wire grounding a~~line connecting the first electrode structure ~~shared between~~, which is common to said first and said second spin transistors, to ground;

a second and a third ~~wires connecting a~~line connected to the second electrode structure of said first spin transistor and ~~a~~the second electrode structure of said second spin transistor, respectively; and

a fourth ~~wire connecting a~~line connected to the third electrode structure of said first spin transistor and ~~a~~the third electrode structure of said second spin transistor.

32. A memory circuit comprising:

a plurality of spin transistors according to claim 16 arra~~y~~nged in a matrix;

~~a first wire sharing and grounding said~~a first line commonly connecting to ground the first electrode structures of a plurality of spin transistors arranged in a first row and the first electrode structures~~, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction and in the row of a plurality of second spin transistors arrayed in the row direction adjacent to the row of said first spin transistors in the column direction;~~ of a plurality of spin transistors arranged in an adjacent, second row;

~~a first bit line sharably connecting said second electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction, and a second bit line sharably connecting said second electrode structures in the row of second spin transistors adjacent to the row of said first spin transistors in the column direction; and~~

a first bitline commonly connecting the second electrode structures of a plurality of spin transistors arranged in a first row and the second electrode structures of a plurality of spin transistors arranged in a second row adjacent to said first row in the column direction;

a second bitline commonly connecting the second electrode structures of said spin transistor in said first row and the second electrode structures of said second spin transistors in said second row adjacent to said first row in the column direction; and

~~a word line sharably~~a wordline commonly connecting the third electrode structures~~,~~ of said plurality of spin transistors~~, in the column of a plurality of spin transistors arrayed in the~~ in a column direction.

33. A memory circuit comprising:

a plurality of spin transistors according to claim 16 arraynged in a matrix;

~~a plurality of first wires sharing and grounding said first electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction and in the row of a plurality of second spin transistors arrayed in the row direction adjacent to the row of said first spin transistors in the column direction, one first wire being provided every two rows;~~

~~a plurality of first bit lines sharably connecting said second electrode structures, of said plurality of spin transistors, in the row of a plurality of first spin transistors arrayed in the row direction, one first bit line being provided every two rows of said spin transistors, and a plurality of second bit lines sharably connecting said second electrode structures in the row of second spin transistors adjacent to the row of said first spin transistors in the column direction, one second bit line being provided every two rows of said spin transistors; and~~

a plurality of first lines each commonly connecting to ground said first electrode structures of a plurality of spin transistors in a first row and those of a plurality of spin transistors in a second row adjacent to said first row in the column direction, wherein each of said first lines is provided for every two rows;

a plurality of first bitlines each commonly connecting said second electrode structures of a plurality of said spin transistors arranged in a first row, wherein each of said first bitlines is provided for every two rows;

a plurality of second bitlines each commonly connecting the second electrode structures of a plurality of spin transistors arranged in a second row adjacent said first row in the column direction, wherein one such second bitline is provided for every two rows of said spin transistors; and

a plurality of ~~word lines sharably~~wordlines commonly connecting the third electrode structures~~, of said plurality of spin transistors, in the column~~ of a plurality of said spin transistors arraynged in the column direction.

34. The ~~storage device~~memory element according to claim 20, wherein information is written by reversing the magnetization in said free layer by a magnetic field induced by ~~flowing electric currents to~~causing a current to flow through said second ~~wire~~line or said third ~~wire~~line with which ~~any one of~~ said first ~~another wire and~~separate line or said second ~~another wire is~~separate line have been replaced ~~and~~, or through said first ~~another wire or said second another wire which is not replaced with these inverts the magnetization of said free layer to change~~separate line or said second separate line that has not been replaced thereby, thus changing the relative magnetization ~~state of~~configuration between said pin layer and said free layer ~~for rewriting information~~.

35. The memory circuit according to claim 27, wherein information is written by causing the relative magnetization configuration between said free layer and said pin layer to be changed by a magnetic field induced by ~~flowing electric currents to said word line~~causing a current to flow through said wordline or said ~~bit line~~bitline with which ~~any one of~~ said first ~~another wire and~~separate line or said second ~~another wire is replaced and~~separate line have been replaced, or through said first ~~another wire or said second another wire which is not~~

~~replaced with these changes the relative magnetization state of said free layer and said pin layer for rewriting information~~separate line or said second separate line that has not been replaced thereby.

ABSTRACT

~~There are provided a~~A spin transistor ~~having~~comprises a spin injector for injecting, ~~as hot carriers, carriers having~~from a first nonmagnetic electrode carriers with a spin parallel to ~~the~~a spin band ~~constituting~~forming the band edge of a first ferromagnetic barrier layer ~~from a first nonmagnetic electrode into~~, to a second nonmagnetic electrode layer ~~and~~, as hot carriers. It also comprises a spin analyzer ~~conducting, by the~~whereby, due to spin -splitting at the band edge of a second ferromagnetic barrier layer, the ~~hot carriers~~spin-polarized hot carriers are transported to a third nonmagnetic electrode when the direction of the spin of the ~~spin-polarized hot~~ carriers injected into the second nonmagnetic electrode is parallel to ~~the direction~~that of the spin of the spin band at the band edge of the second ferromagnetic barrier layer ~~and not conducting the hot carriers~~, whereas the hot carriers are not transported to the third nonmagnetic electrode ~~when they are anti-parallel, and a storage device using the~~in the case of antiparallel spin. A memory element is also provided that comprises such a spin transistor.